FILE 'HCAPLUS, INSPEC, JICST-EPLUS, INSPHYS, COMPENDEX, CEABA-VTB' 14:00:47 ON 02 JUL 2002
L1 3 S SUPERJUNCTION DEVICES/TI AND SIMULATED/TI

FILE 'HCAPLUS' ENTERED AT 14:02:00 ON 02 JUL 2002
L3 1 S L***

FILE 'HCAPLUS, INSPEC, JICST-EPLUS, INSPHYS, COMPENDEX, CEABA-VTB' 14:02:03 ON 02 JUL 2002
L*** DEL SEL L1 1 5 : 1 TERM

FILE 'HCAPLUS' ENTERED AT 14:02:29 ON 02 JUL 2002
L5 1 S L***

FILE 'HCAPLUS, INSPEC, JICST-EPLUS, INSPHYS, COMPENDEX, CEABA-VTB, WPIX, JAPIO, NTIS' ENTERED
L6 670 S FUJIHIRA T?/AU,IN
L7 1513 S MIYASAKA Y?/AU,IN
L8 20 S L6 AND L7
L9 13 DUP REM L8 (7 DUPLICATES REMOVED)
L10 0 S L9 AND LATERAL?
L11 6 S L9 AND SUPER###############
L12 3 S (US4754310 OR US5216275)/PN
L13 200 S INTERNATIONAL RECTIFIER?/PA,CS
L14 152 S KINZER D?/AU,IN
L15 27 S SRIDEVAN S?/AU,IN
L16 32 S L13 AND L14
L17 3 S L13 AND L15
L18 3 S L14 AND L15
L19 4 S (L17 OR L18)
L*** DEL SEL L19 1 2 : 1 TERM

FILE 'HCAPLUS' ENTERED AT 14:17:19 ON 02 JUL 2002
L21 1 S L***

FILE 'HCAPLUS, INSPEC, JICST-EPLUS, INSPHYS, COMPENDEX, CEABA-VTB, WPIX, JAPIO, NTIS' ENTERED AT 14:18:23 ON 02 JUL 2002
L22 7 S (US 6103578 OR US 4855804 OR US 6184555)/PN

FILE 'DPCI' ENTERED AT 14:23:13 ON 02 JUL 2002
L23 59 S (GB2089119 OR EP53854 OR EP053854 OR JP57124469 OR DE3173754 OR US4754310 OR CN1056018 OR US5216275)/PN.D
L24 SEL L23 1- PRN : 76 TERMS

FILE 'HCAPLUS, INSPEC, JICST-EPLUS, INSPHYS, COMPENDEX, CEABA-VTB, WPIX, JAPIO, NTIS' ENTERED
L25 136 S L24
L26 2 S L25 AND (SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L27 11 S L25 AND TRENCHES
L28 11 S L27 NOT L26
L29 21 S L25 AND LATERAL##
L30 7 S (L29 AND (JUNCTION OR HOMOJUNCTION OR HETEROJUNCTION)) NOT (L27 OR L26)
L31 131 S (SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L32 134 S SUPER HOMOJUNCTION OR SUPER HETEROJUNCTION OR L31
L33 15 S L32 AND LATERAL##
L34 6336 S SIDE##(4A)(SUPERJUNCTION OR JUNCTION OR HETEROJUNCTION OR HOMOJUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)

FILE 'SCISEARCH' ENTERED AT 14:33:41 ON 02 JUL 2002
L35 9 S ("FUJIHIRA T, 1998, P423, ISPSD"/RE OR "FUJIHIRA T, 1998, P423, P ISPSD"/RE OR "FUJIHIRA T, 1998, P423, P ISPSD 98"/RE OR "FUJIHIRA T, 1998, P493, P 11 ISPID IEEE"/RE)
L36 2 S "FUJIHARA T, 1998, P423, P INT S POW SEM DEV"/RE
L37 11 S (L35 OR L36)
L38 66 S RESURF
L39 39 S L38 AND (SEMICONDUCT? OR MOS OR MOSFET OR FIELD EFFECT OR JUNCTION OR SUPERJUNCTION OR TRENCH)
L40 3 S L39 AND TRENCH
L41 17 S REDUCED SURFACE FIELD
L42 1 S L41 AND TRENCH
L43 16 S L41 AND (SEMICONDUCT? OR LDMOS OR LDMOSFET OR TRANSISTOR OR MOS OR MOSFET OR FIELD EFFECT OR JUNCTION OR SUPERJUNCTION OR TRENCH)
L44 1 S L41 AND (SUPERJUNCTION OR JUNCTION OR HETEROJUNCTION OR HOMOJUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L45 8 S L41 AND LATERAL##
L46 7 S L45 NOT (L40 OR L44)

FILE 'HCAPLUS, INSPEC, JICST-EPLUS, INSPHYS, COMPENDEX, CEABA-VTB, WPIX, JAPIO, NTIS' ENTERED AT 14:42:03 ON 02 JUL 2002

L47 4372 S SHALLOW####(2A) TRENCH
L48 1941 S LATERAL##(4A)(SUPERJUNCTION OR JUNCTION OR HETEROJUNCTION OR HOMOJUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L49 8235 S L34 OR L48
L50 6 S L49 AND L47
L51 5 S LATERAL##(4A)(SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L52 1 S SIDE##(4A)(SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L53 26 S L22 OR L26 OR L28 OR L30
L54 32 S L53 OR L50
L55 12 S (L50 OR L51 OR L52)
L56 22 S L33 OR L55
L57 16 S L56 NOT L54
L58 10 DUP REM L57 (6 DUPLICATES REMOVED)
L59 12601 S (L34 OR (L47 OR L48 OR L49))
L60 1036 S L59 AND TRENCHES
L61 139 S L60 AND (WAFER OR CHIP)
L62 21 S L61 AND (CONDUCTIVITY TYPE OR "P" OR "N")
L63 9 S L61 AND EXTEND#####
L64 1 S L61 AND RECEIVING
L65 5 S L61 AND SPACED
L66 10 S L61 AND DIFFUSION
L67 2 S L61 AND LATERAL##
L68 16 S L61 AND SIDE##
L69 5 S L61 AND WALLS
L70 3 S L61 AND (CONCENTRATION OR DOSE)
L71 5 S L61 AND MESA
L72 0 S L61 AND PILLAR####
L73 2 S L61 AND GATE ELECTRODE
L74 0 S L61 AND (MOSGATE## OR MOS GATE##)
L75 2 S L61 AND GATE STRUCTURE
L76 9 S L61 AND (MOS OR METAL OXIDE OR LDMOS)
L77 29 S L61 AND THICKNESS
L78 0 S L61 AND (BV OR DEPLET###### OR BLOCK###(2A) (VOLT##### OR POTENTIAL OR "V"))
L79 18 S (SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION) AND (BV OR DEPLET#### ## OR BLOCK###(2A)(VOLT##### OR POTENTIAL OR "V"))
L80 11435 S (JUNCTION OR HOMOJUNCTION OR HETEROJUNCTION) AND (BV OR DEPLET###### OR BLOCK###(2A)(VOLT##### OR POTENTIAL OR "V"))
L81 910 S SWITCH### AND (HIGHSIDE OR LOWSIDE OR (HIGH OR LOW)(W) SIDE)
L82 557 S RESURF OR REDUCED SURFACE FIELD
L83 11840 S LIGHTLY DOPED
L84 346 S RAIL VOLTAGE
L85 7 S TRENCH RECEIVING
L86 1491 S DIELECTRIC FILL###
L87 48 S L56 OR L54
L88 98 S (L62 OR L63 OR L64 OR L65 OR L66 OR L67 OR L68 OR L69 OR L70 OR L71 OR L72 OR L73 OR L74 OR L75 OR L76 OR L77 OR L78 OR L79) OR L85
L89 5 S L80 AND L81
L90 29 S L80 AND L82
L91 213 S L80 AND L83
L92 2 S L80 AND L84
L93 0 S L80 AND L85
L94 3 S L91 AND TRENCHES
L95 1 S L90 AND TRENCHES
L96 10 S L81 AND L82
L97 9 S L81 AND L83
L98 1 S L81 AND L84
L99 0 S L81 AND L85
L100 18 S L82 AND L83
L101 0 S L82 AND L84
L102 0 S L82 AND L85
L103 0 S L83 AND L84
L104 0 S L83 AND L85
L105 0 S L100 AND TRENCHES
L106 0 S L100 AND TRENCH
L107 0 S L100 AND (SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L108 77 S L89 OR L90 OR (L92 OR L93 OR L94 OR L95 OR L96 OR L97 OR L98 OR L99 OR L100)
L109 170 S L88 OR L108
L110 164 S L109 NOT L87
L111 81 S L110 AND TRENCHES
L112 1 S L111 AND (SUPER OR SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L113 13 S L110 AND (SUPER OR SUPERJUNCTION OR SUPER JUNCTION OR SUPERHOMOJUNCTION OR SUPERHETEROJUNCTION)
L114 9 S L110 AND (LATERAL## OR SIDE##)(8A)(JUNCTION OR HOMOJUNCTION OR HETEROJUNCTION)
L115 22 S (L113 OR L114)

L19 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:450058 HCAPLUS
TI High voltage vertical conduction superjunction semiconductor device
IN **Kinzer, Daniel M.**; Sridevan, Srikant
PA **International Rectifier** Corporation, USA
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01L029-78
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002047171	A1	20020613	WO 2001-US47275	20011203
PRAI	US 2000-732401	A	20001207		

AB A high voltage vertical conduction semiconductor device has a plurality of deep trenches or holes in a lightly doped body of 1 cond. type. A diffusion of the other cond. type is formed in the trench walls to a depth and a concn. which matches that of the body so that, under reverse blocking, both regions fully deplete. The elongated trench or hole is filled with a dielec. which may be a composite of nitride and oxide layers having a lateral dimension change matched to that of the Si. The filler may be a highly resistive semi-insulating poly-Si which permits leakage current flow from source to drain to ensure a uniform elec. field distribution along the length of the trench during blocking.

L19 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:833823 HCAPLUS
DN 135:365346
TI Angle implant process for cellular deep trench sidewall doping
IN Ren, Lipping; **Sridevan, Srikant**
PA **International Rectifier** Corp., USA
SO U.S. Pat. Appl. Publ., 5 pp.
CODEN: USXXCO
DT Patent
LA English
IC H01L021-8238
NCL 438200000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001041400	A1	20011115	US 2001-852579	20010510
	DE 10123616	A1	20020124	DE 2001-10123616	20010515
	JP 2002110693	A2	20020412	JP 2001-145290	20010515
PRAI	US 2000-204033P	P	20000515		
	US 2001-852579	A	20010510		

AB A process is described for making a superjunction semiconductor device. A large no. of sym. spaced trenches penetrate the N- epitaxial layer of Si atop an N+ body to a depth of 35-40 .mu.m. The wells have a circular cross-section and a diam. of .apprx.9 .mu.m. The trench walls are implanted by an ion implant beam of B which is at a slight angle to the axis of the trenches. The wafer is intermittently or continuously rotated about an axis <90.degree. to its surface to cause skewing of the implant beam and more uniform distribution of B ions over the interior surfaces of the trenches.

L19 ANSWER 4 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2001-365964 [38] WPIX
DNN N2001-266880
TI Power MOSFET has polycrystalline silicon carbide on substrate with resistivity varying with respective groove walls and diffusion layer along bottom surface of grooves.
DC U12
IN **KINZER, D M; SRIDEVAN, S**
PA (INRC) INT RECTIFIER CORP
CYC 1
PI US 6194741 B1 20010227 (200138)* 8p H01L031-0312
ADT US 6194741 B1 US 1998-185110 19981103
PRAI US 1998-185110 19981103
IC ICM H01L031-0312
AB US 6194741 B UPAB: 20010711
NOVELTY - A gate insulating layer (31) is formed along the walls of U-shaped grooves (30) in the N+ type substrate (21). Polycrystalline silicon carbide is distributed on the substrate such that resistivity of carbide decreases and increases in parallel and perpendicular to vertical walls of grooves, respectively. P-type diffusion layer (32) extends along the bottom surface of the groove.

DETAILED DESCRIPTION - A channel of depth less than the grooves is formed on the substrate. A source region of depth less than the channel depth is formed on the substrate. A gate insulation layer is disposed within the grooves. Conductive polysilicon gate is filled in the grooves in isolation from the grooves. Drain contact and gate contact are connected to the substrate and polysilicon gate.

USE - Power MOSFET.

ADVANTAGE - Improves high channel mobility as the grooves are effectively insulated. Protects gate insulating film from the electrostatic field under heavy stress, by forming depletion layer below grooves. Reduces dielectric breakdown of gate insulating film by providing diffusion layer below grooves.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of power MOSFET using U-shaped trench.

N+ type substrate 21
U-shaped grooves 30
Gate insulating layer 31
P-type diffusion layer 32

L58 ANSWER 5 OF 10 INSPEC COPYRIGHT 2002 IEE DUPLICATE 3
AN 2001:7092177 INSPEC DN B2001-12-2560R-130
TI **Lateral** unbalanced **super junction** (USJ)/3D-RESURF for high breakdown voltage on SOI.
AU Ng, R.; Udrea, F.; Sheng, K. (Dept. of Eng., Cambridge Univ., UK); Ueno, K.; Amaratunga, G.A.J.; Nishiura, M.
SO Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216)
Tokyo, Japan: Inst. Electr. Eng. Japan, 2001. p.395-8 of xxxi+467 pp. 12 refs. Also available on CD-ROM in PDF format
Conference: Osaka, Japan, 4-7 June 2001
Sponsor(s): Inst. Electr. Eng. Japan
ISBN: 4-88686-056-7
DT Conference Article
TC New Development; Theoretical
CY Japan
LA English
AB This paper examines for the first time the possibility of the **Super Junction** (SJ) concept to realise **lateral** device structures on SOI with high breakdown voltage and low on-resistance for use in power integrated circuits (PICs). More specifically, a novel structure based on an unbalanced SJ (USJ) configuration is proposed and investigated using the 3D-device simulator, DAVINCI. The physics of the SJ related structure is described in detail and is shown to rely on a truly three dimensional RESURF effect to achieve high voltage blocking capability-hence the acronym 3D-RESURF. It is also shown that a suitable choice of n and p stripe geometry, enables breakdown voltage in excess of 600 volts to be realised on SOI technology with 4 mu m of buried oxide (BOX). Methods for optimising the breakdown capability of the proposed structure are also presented.

L58 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 2
AN 2002:205362 HCAPLUS
DN 136:302344
TI **Lateral** smart-discrete process and devices based on thin-layer silicon-on-insulator
AU Letavic, T.; Petruzzello, J.; Simpson, M.; Curcio, J.; Mukherjee, S.; Davidson, J.; Peake, S.; Rogers, C.; Rutter, P.; Warwick, M.; Grover, R.
CS Philips Research USA, Briarcliff Manor, NY, 10510, USA
SO ISPSD'01, Proceedings of the International Symposium on Power Semiconductor Devices and ICs, 13th, Osaka, Japan, June 4-7, 2001 (2001), 407-410 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 69CIIB; ISBN: 4-88686-056-7
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB A ten-mask **lateral** smart-discrete process technol. which combines novel high-voltage RESURF transistor structures and a merged bipolar/DMOS process flow on thin-layer SOI substrates is presented. Benchmarking shows that 650 V/1.2 .OMEGA. SOI **lateral** smart-discrete devices exhibit a total gate charge which is a factor-of-two lower than vertical **super-junction** devices, a temp.-independent body diode reverse recovery time which is a factor-of-two smaller than vertical ultra-fast Si diodes, and total hard-switching losses which are lower than conventional VDMOS. The total gate charge, reverse recovery time, and switching delay times are the lowest reported values for 650 V Si devices. This, in conjunction with a process with integrated logic, establishes SOI smart-discrete technol. as best-in-class for efficient high-frequency power conversion.

L58 ANSWER 6 OF 10 INSPEC COPYRIGHT 2002 IEE DUPLICATE 4
AN 2001:7092110 INSPEC DN B2001-12-2560P-012
TI Ultra-high voltage device termination using the 3D RESURF (**super -junction**) concept - experimental demonstration at 6.5 kV.
AU Udrea, F.; Trajkovic, T. (Dept. of Eng., Cambridge Univ., UK); Thomson, J.; Coulbeck, L.; Waind, P.R.; Amaratunga, G.A.J.; Taylor, P.
SO Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216)
Tokyo, Japan: Inst. Electr. Eng. Japan, 2001. p.129-32 of xxxi+467 pp. 8 refs. Also available on CD-ROM in PDF format
Conference: Osaka, Japan, 4-7 June 2001
Sponsor(s): Inst. Electr. Eng. Japan
ISBN: 4-88686-056-7
DT Conference Article
TC New Development; Experimental
CY Japan
LA English
AB We propose here and experimentally demonstrate a novel breakdown termination termed The 3D-RESURF Termination that can be applied to a large class of high to ultra-high voltage devices, such as diodes, thyristors, IGBTs, etc. The novel termination is based on the 3D RESURF concept (**lateral super-junction**) proposed by us and others for **lateral** integrable devices. We have fabricated vertical diodes and IGBTs rated at 6.5 kV and demonstrated that the use of 3D RESURF p and n layers placed between adjacent p+ floating rings resulted in maximum breakdown voltage (6.5 kV). This is 2.5 kV larger than the breakdown voltage obtained from a standard field ring terminated device fabricated side by side on the same chip. Moreover, the 3D-RESURF edge termination uses a total length of 1 mm, which is only 60% of standard 6.5 kV JTE terminations. This results in area saving of up to 40%, depending on the active area of the chip.

L115 ANSWER 3 OF 22 INSPEC COPYRIGHT 2002 IEE
AN 2001:7092184 INSPEC DN B2001-12-2560R-137
TI Shallow angle implantation for extended trench gate power MOSFETs with **super junction** structure.
AU Hattori, Y.; Suzuki, T.; Kodama, M.; Hayashii, E.; Uesugi, T. (Toyota Central Res. & Dev. Labs. Inc., Aichi, Japan)
SO Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216)
Tokyo, Japan: Inst. Electr. Eng. Japan, 2001. p.427-30 of xxxi+467 pp. 4 refs. Also available on CD-ROM in PDF format
Conference: Osaka, Japan, 4-7 June 2001
Sponsor(s): Inst. Electr. Eng. Japan
ISBN: 4-88686-056-7
DT Conference Article
TC New Development; Experimental
CY Japan
LA English
AB In this paper, we present a new deep trench power MOSFET with **super junction** structure in the drift region, which exhibits strongly improved a relationship between **blocking voltage** and on-resistance. An accurate control of impurity concentration of n drift region in the trench sidewall is important to achieve the proposed MOSFET. Thus, we also quantitatively analyzed shallow angle ion implantations into trench sidewall by using a macrosize trench model. It was found that 40% ions doped into the incident sidewall and 12% ions were re-implanted into the opposite sidewall at the incident angle of 10 degrees.

L115 ANSWER 4 OF 22 INSPEC COPYRIGHT 2002 IEE
AN 2001:7001995 INSPEC DN B2001-09-2560R-035
TI Oxide-bypassed VDMOS (OBVDMOS): an alternative to **superjunction** high voltage MOS power devices.
AU Liang, Y.C.; Gan, K.P.; Samudra, G.S. (Dept. of Electr. & Comput. Eng., Nat. Univ. of Singapore, Singapore)
SO IEEE Electron Device Letters (Aug. 2001) vol.22, no.8, p.407-9. 14 refs.
Doc. No.: S0741-3106(01)06641-1
Published by: IEEE
Price: CCCC 0741-3106/2001/$10.00
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200108)22:8L.407:OBVO;1-0
DT Journal
TC Practical; Theoretical; Experimental
CY United States
LA English
AB The **superjunction** concept has been proposed to overcome the ideal silicon MOSFET limit, but its fabrication was handicapped by the precise charge balance requirement and inter-diffusion problem. We report a novel device structure termed oxide-bypassed VDMOS (OBVDMOS) that requires the well-established oxide thickness control instead of the difficult doping control in translating the limit to a higher **blocking voltage**. This is done by using metal-thick-oxide (MTO) at the sidewalls of drift region. One can choose to have a higher **blocking voltage** or increase the background doping. A PiN structure, essentially identical to MOSFET during off state, was fabricated to demonstrate the proposed concept. Its measured BVdss of 170 V is 2.5 times higher than measured conventional device BVdss of 67 V on the same silicon wafer.
CC B2560R Insulated gate field effect transistors; B2560P Power

L58 ANSWER 2 OF 10 WPIX (C) 2002 THOMSON DERWENT
AN 2002-242963 [30] WPIX
DNN N2002-187883
TI **Lateral** semiconductor device e.g. **lateral** **super-junction** MOSFET, has loop layer formed of zones of alternating conductivity types.
DC U12
IN FUJIHARA, T; IWAMOTO, S; ONISHI, Y; SATO, T; FUJIHIRA, T
PA (FJIE) FUJI ELECTRIC CO LTD; (FUJI-I) FUJIHIRA T; (IWAM-I) IWAMOTO S; (ONIS-I) ONISHI Y; (SATO-I) SATO T
CYC 3
PI DE 10120030 A1 20011031 (200230)* 21p H01L029-06
JP 2001308324 A 20011102 (200230) 12p H01L029-78
US 2001050394 A1 20011213 (200230) H01L029-76
PRAI JP 2000-127021 20000427
IC ICM H01L029-06; H01L029-76; H01L029-78
ICS H01L029-739; H01L029-861
AB DE 10120030 A UPAB: 20020513
NOVELTY - The **lateral** semiconductor device includes a layer (12) of alternating conductivity type arranged between two main electrodes on the main surface of a semiconductor chip. The layer comprises first zones (1) of a first conductivity type and second zones (2) of a second conductivity type, and forms a closed loop surrounding one of the main electrodes.

USE - The device may comprise a MOSFET, bipolar transistor, IGBT or diode.

ADVANTAGE - Higher breakdown voltage.

DESCRIPTION OF DRAWING(S) - The drawing shows a plan of an n-channel **lateral** SJ-MOSFET.

Layer of alternating conductivity type 12

Dwg.1/13

L1 ANSWER 3 OF 3 COMPENDEX COPYRIGHT 2002 EEI
AN 1998(51):4429 COMPENDEX
TI **Simulated** superior performances of semiconductor **superjunction devices.**
AU Fujihira, Tatsuhiko (Fuji Electric Co, Ltd, Matsumoto, Jpn); Miyasaka, Yasushi
MT Proceedings of the 1998 10th International Symposium on Power Semiconductor Devices & ICs, ISPSD'98.
MO IEEE
ML Kyoto, Jpn
MD 03 Jun 1998-06 Jun 1998
SO IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD) 1998.IEEE, Piscataway, NJ, USA,98CH36212.p 423-426
CODEN: PISDEK
PY 1998
MN 49128
DT Conference Article
TC Theoretical
LA English
AB Performances of majority- and minority-carrier semiconductor superjunction devices are examined and compared to that of standard devices in terms of forward current density, reverse leakage current, and switching charge.Based on two-dimensional simulations and theoretical calculations, it is shown that two orders of magnitude improvement in forward current density, an order of magnitude improvement in switching charge for majority-carrier superjunction devices, and an order of magnitude improvement in forward current density for minority-carrier superjunction devices are feasible when compared to standard devices.(Author abstract) 11 Refs.
CC 714.2 Semiconductor Devices and Integrated Circuits; 701.1 Electricity: Basic Concepts and Phenomena; 921 Applied Mathematics
CT *Semiconductor junctions; Current density; Leakage currents; Computational methods; Current voltage characteristics; Schottky barrier diodes
ST Semiconductor superjunction devices; Reverse leakage currents

L5 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN **1997:722924** HCAPLUS
TI Theory of semiconductor superjunction devices
AU Fujihira, Tatsuhiko
CS Matsumoto Factory, Fuji Electric Co., Ltd., Matsumoto, 390, Japan
SO Jpn. J. Appl. Phys., Part 1 (1997), 36(10), 6254-6262
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A new theory of semiconductor devices, called "semiconductor superjunction (SJ) theory", is presented. To overcome the trade-off relationship between breakdown voltage and on-resistance of conventional semiconductor devices, SJ devices utilize a no. of alternately stacked, p- and n-type, heavily doped, thin semiconductor layers. By controlling the degree of doping and the thickness of these layers, according to the SJ theory, this structure operates as a pn junction with low on-resistance and high breakdown voltage. Anal. formulas for the ideal specific on-resistance and the ideal breakdown voltage of SJ devices are theor. derived. Anal. based on the formulas and device simulations reveals that the on-resistance of SJ devices can be reduced to less than 10-2 that of conventional devices.

L12 ANSWER 3 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 1982-H0506E [24] WPIX
TI HV semiconductor device - comprises body with depletion layer throughout portion and two types of conductivity layer interleaved with one another.
DC U12
IN COE, D J
PA (PHIG) PHILIPS ELTRN & ASSOC IND LTD
CYC 7
PI GB 2089119 A 19820616 (198224)* 16p
EP 53854 A 19820616 (198225) EN
R: DE FR GB IT NL
JP 57124469 A 19820803 (198236)
EP 53854 B 19860205 (198606) EN
R: DE FR GB IT NL
DE 3173754 G 19860320 (198613)
US 4754310 A 19880628 (198828) <--
ADT EP 53854 A EP 1981-201293 19811123; US 4754310 A US 1984-678365 19841204
PRAI GB 1980-39499 19801210
REP 2.Jnl.Ref; US 3925803
IC H01L029-06
AB GB 2089119 A UPAB: 19930915
A field-effect transistor, bipolar transistor, PIN diode, Schottky rectifier or other high voltage semiconductor device comprises a semiconductor body (1) throughout a portion (3) of which a depletion layer is formed in at least a high voltage mode of operation of the device, for example by reverse biasing a rectifying junction (5). The known use of a single high-resistivity body portion of one conductivity type both to carry the high-voltage and to conduct current results in the series resistivity increasing approximately in proportion with the square of the breakdown voltage.

This square-law relationship is avoided by using a depleted body portion (3) which comprises an interleaved structure of two regions (11,12) of alternating conductivity types which carry the high voltage occuring across the depeleted body portion (3).

The thickness and doping concentration of each of these two regions (11,12) are such that when depleted the space charge per unit area formed in each is balanced at least to the extent that an electric field resulting from any imbalance is less than the critical field strength at which avalanche breakdown would occur in the body portion (3).

1
ABEQ EP 53854 B UPAB: 19930915
A high voltage semiconductor device comprising a semiconductor body and means for forming a depletion layer throughout a portion of said body in at least a high voltage mode of operation of the device, characterised in that said body portion comprises a plurality of first regions of a first conductivity type interleaved with second regions of the opposite, second conductivity type, the total number of first and second regions being at least four, in that said first and second regions have a sufficient length perpendicular to their thickness for carrying a voltage in excess of 100 volts across said body portion when depleted of free charge-carriers by the depletion layer spreading therein at least in the high voltage mode of operation of the device, in that at least said first regions in at least one mode of operation of the device provide electrically parallel current paths extending through said body portion, and in that the thickness and doping concentration of each of said first and second regions is such that, when depleted of free charge-carriers and carrying said voltage in excess of 100 volts, said first and second regions form interleaved positive and negative space charge regions the space charge per unit area of which is balanced at least to such an extent that the electric field resulting from said space charge is less than the critical field strength at which avalanche breakdown would occur in said body portion. The device comprises a semiconductor body having a depletion layer formed

throughout a portion in at least a high voltage mode of operation of the device, such as, by reverse biasing a rectifying junction. A single high-resistivity body portion of one conductivity type carries both the high voltage and to conduct current results in a series resistivity increasing approximately in proportion with the square of the breakdown voltage. The square-law relationship is avoided by a depleted body portion comprising an interleaved structure of two regions of alternating conductivity types carries the high voltage which occurs across the depleted body portion.

The thickness and doping concentration of each of these regions are such that when depleted the space charge per unit area formed in each of these regions is balanced at least to the extent that an electric field resulting from any imbalance is less than the critical field strength at which avalanche breakdown would occur in the body portion. The first regions in at least one mode of operation of the device provide electrically parallel current paths extending thorugh the body portion.

USE - FET, bipolar transistor, PIN diode, Schottky rectifier etc.

(18pp)

4754310A

ABEQ US 4754310 A UPAB: 19930915

The device comprises a semiconductor body having a depletion layer formed throughout a portion in at least a high voltage mode of operation of the device, such as, by reverse biasing a rectifying junction. A single high-resistivity body portion of one conductivity type carries both the high voltage and to conduct current results in a series resistivity increasing approximately in proportion with the square of the breakdown voltage. The square-law relationship is avoided by a depleted body portion comprising an interleaved structure of two regions of alternating conductivity types carries the high voltage which occurs across the depleted body portion.

The thickness and doping concentration of each of these regions are such that when depleted the space charge per unit area formed in each of these regions is balanced at least to the extent that an electric field resulting from any imbalance is less than the critical field strength at which avalanche breakdown would occur in the body portion. The first regions in at least one mode of operation of the device provide electrically parallel current paths extending thorugh the body portion.

USE - FET, bipolar transistor, PIN diode, Schottky rectifier etc.

FS EPI

FA AB

MC EPI: U12-C; U12-D; U12-E01

L12 ANSWER 2 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 1992-259643 [32] WPIX
TI Power semiconductor device - has two kinds of conducting materials alternately arranged to form composite buffer layer-depletion zone NoAbstract.
DC U12
IN CHEN, X
PA (UYEL-N) UNIV ELECTRONIC SCI & TECHNOLOGY
CYC 2
PI CN 1056018 A 19911106 (199232)* H01L029-38
US 5216275 A 19930601 (199323)B 10p H01L029-76 <--
ADT CN 1056018 A CN 1991-101845 19910319; US 5216275 A US 1991-761407 19910917
PRAI CN 1991-101845 19910319
IC ICM H01L029-38; H01L029-76
ICS H01L029-70; H01L029-78
ABEQ US 5216275 A UPAB: 19931115
The semiconductor power device has the voltage across the p+ region(s) and the n+ region(s) sustained by a composite buffer layer, shortly as CB-layer. The CB-layer contains two kinds of semiconductor regions with opposite types of conduction. The two kinds of regions are alternatively arranged, viewed from any cross section parallel to the interface between the layer itself and the n+ (or p+) region.

ADVANTAGE - Relation between on-resistance in unit area Ron and breakdown voltage VB of the CB-layer is Ron ocVB power 113 which represents a breakthrough to conventional voltage sustaining layer, whereas other performances of the power devices remain almost unchanged.

Dwg.3/9
FS EPI
FA AB
MC EPI: U12-D02A; U12-E01

L50 ANSWER 6 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 1995-105517 [14] WPIX
DNN N1995-083436 DNC C1995-048191
TI Photovoltaic micro-array structure and method - eliminates need for semi-insulating substrate support by using filled isolation trenches in monolithic construction.
DC A85 L03 U12 X15
IN CAVICCHI, B T; KRUT, D D; MICHAELS, D E
PA (SPEC-N) SPECTROLAB INC
CYC 1
PI US 5391236 A 19950221 (199514)* EN 7p H01L031-05
ADT US 5391236 A US 1993-99756 19930730
PRAI US 1993-99756 19930730
IC ICM H01L031-05
ICS H01L031-18
AB US 5391236 A UPAB: 19950412
A method of forming a pair of mutually isolated photovoltaic cells on a bulk semiconductor substrate (4) having a pn **junction** (8) at its front **side** (6), comprises forming substrate contacts to cell area and forming a trench partly into the substrate between solar cell areas. The trench is filled with an adhering insulating filler (16), a second trench formed into the substrate from the opposite side (32) to form an insulating continuum between cells, and front contacts formed to the cell areas (22).

Also claimed is a method as above of forming a photovoltaic cell array comprising forming wide **shallow trenches** from the front of the substrate and narrow and deeper inner trenches from these, filling the inner trenches, forming contacts, and forming a pattern of back trenches extending to the filled trenches to isolate adjacent cells.

Further claimed is a photovoltaic cell array formed as above.

Also claimed is an array as above having a trench network through the substrate filled to half the thickness with filler to maintain mechanical integrity.

Further claimed is an array as above having the wider and narrower trenches as above.

Also claimed is a monolithic photovoltaic structure as above having front and back contacts, shaped trenches, and with the resistance of the bulk semiconductor between the back contact lead and electrode being low enough to give a contact path, and with the cells being connected in series.

USE - For solar cell arrays, power converter from fibre optic systems, and on/off switches.

ADVANTAGE - The need for a semi-insulating substrate is eliminated, high mechanical strength is achieved, and the size and cost of the array are reduced.

Dwg.1G/2
FS CPI EPI

L50 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:167127 HCAPLUS
DN 132:201897
TI Process to reduce defect formation occurring during **shallow trench** isolation formation
IN Chang, Jung-Ho; Chen, Hsi-Chuan; Lin, Dahcheng
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-76
NCL 438426000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6037238	A	20000314	US 1999-224717	19990104

AB A process for creating an insulator-filled **shallow trench** isolation region in a semiconductor substrate features the use of a high-temp. H anneal, performed after an anisotropic RIE procedure used to create the **shallow trench** shape in the substrate. The high-temp. H anneal repairs defects in the substrate created by the **shallow trench** RIE procedure, and also creates a denuded zone at or near the **shallow trench** shape. The defect-free denuded zone acts as a uniform insulating trench liner, and also allows a min. of junction leakage to occur in the region where a source/drain-substrate **junction** is butted against the **side** of the insulator-filled **shallow trench**.

L50 ANSWER 3 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2001-233682 [24] WPIX
DNN N2001-166912 DNC C2001-069992
TI Manufacturing method of the borderless contact - with the capability of increasing the contact area between the contact and the connection points of the device such that a lower resistance can be obtained between the device and t.
DC L03 U11
IN CHEN, W; SHIU, S
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI TW 411572 A 20001111 (200124)* H01L021-768
ADT TW 411572 A TW 1999-106104 19990416
PRAI TW 1999-106104 19990416
IC ICM H01L021-768
AB TW 411572 A UPAB: 20010502
NOVELTY - A manufacturing method of the borderless contact. The **shallow trench** isolation structure containing the first oxide layer, the layer of nitride material and the second oxide layer on the substrate. By removing part of the second oxide layer and the layer of nitride material, a recess is formed at the **shallow trench** isolation structure such that part of the substrate is exposed at the sidewall of the recess. After forming the transistor structure on the substrate, the sidewall formed on the recess of the substrate has deeper **junction** depth so that the **side** source/drain region is exposed. The layer of metal silicide is formed on the surface of the gate and the source/drain region. Then, the inter-layer dielectrics are formed to cover the substrate and additionally, the borderless contact is formed on the inter-layer dielectrics.
Dwg.1/1
FS CPI EPI

L50 ANSWER 4 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2000-505496 [45] WPIX
DNN N2000-373819 DNC C2000-151636
TI Formation of integrated circuit using dual salicidation process to form silicide gate conductor to greater thickness than junction silicide structure.
DC L03 U11
IN FULFORD, H J; GARDNER, M I; MAY, C E
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6100173 A 20000808 (200045)* 10p H01L021-3205
ADT US 6100173 A US 1998-116066 19980715
PRAI US 1998-116066 19980715
IC ICM H01L021-3205
AB US 6100173 A UPAB: 20000918
NOVELTY - The method comprises

(i) providing a gate dielectric (14) arranged across a semiconductor substrate (10) comprising source **junction laterally** spaced from a drain **junction** by a channel region, and a polysilicon gate conductor (24) spaced above the channel region by the gate dielectric, the polysilicon gate conductor being arranged laterally between a pair of dielectric sidewall spacers,

(ii) depositing a first layer of refractory metal across exposed surfaces of the gate dielectric, the sidewall spacers and the gate conductors, and

(iii) heating the first layer of refractory metal to convert the polysilicon gate conductor to a silicide gate conductor (36).

The entire gate conductor comprises silicide. The gate dielectric comprises a thickness sufficient to inhibit silicide from forming upon the source and drain junctions.

USE - Dual salicidation process forming a silicide gate conductor having a greater thickness than silicide structures formed upon source and drain regions.

ADVANTAGE - The silicide structures provide for lower contact resistances between the source and drain regions and contacts formed above the silicide structures.

DESCRIPTION OF DRAWING(S) - The drawing shows a partial cross-section of the semiconductor topography.

Semiconductor substrate 10
Shallow trench isolation structures 12
Gate dielectric 14
Lightly doped drain 18
Sidewall spacers 22
Polysilicon gate conductor 24
Gate conductor 30
Silicide structure 36

Dwg.12/12
FS CPI EPI

L50 ANSWER 5 OF 6 WPIX (C) 2002 THOMSON DERWENT

AN 1996-199693 [20] WPIX

CR 1997-099485 [09]

DNN N1996-167614

TI Lateral resonant tunnelling device having gate electrode aligned with tunnelling barriers - has **shallow trench** etch into smaller band-gap material layer, and refill and overgrowth with larger band-gap materials to form tunnelling barriers having quantum well between.

DC U12

IN JOVANOVIC, D; RANDALL, J N

PA (TEXI) TEXAS INSTR INC

CYC 1

PI US 5504347 A 19960402 (199620)* 18p H01L029-06

ADT US 5504347 A US 1994-323983 19941017

PRAI US 1994-323983 19941017

IC ICM H01L029-06

AB US 5504347 A UPAB: 19970307

The **lateral** tunnelling structure includes a **heterojunction** with semiconductor layer having a band edge offset from the corresp. band edge of an overlying material layer, an electrode on the material layer and at least two tunnelling barriers aligned to edges of the electrode and extends from the layer into but not through the semiconductor layer.

Contacts to the semiconductor layer are remote from the tunnelling barriers. The semiconductor layer is a first group III-V compound, such as silicon, and the material layer is a second group III-V cpd., such as a dielectric.

ADVANTAGE - Provides lateral resonant structures and fabrication methods. Omission of gate simplifies process.Carrier distribution can be more tightly confined at interface by grading composition of well layer.

Dwg.11f/11

FS EPI

L115 ANSWER 19 OF 22 JAPIO COPYRIGHT 2002 JPO
AN 2000-040822 JAPIO
TI **SUPERJUNCTION** SEMICONDUCTOR ELEMENT AND ITS MANUFACTURE
IN FUJIHIRA TATSUHIKO
PA FUJI ELECTRIC CO LTD
PI JP 2000040822 A 20000208 Heisei
AI JP1998-209267 (JP10209267 Heisei) 19980724
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
IC ICM H01L029-78
ICS H01L021-336
AB PROBLEM TO BE SOLVED: To provide a **superjunction** semiconductor element in which in crease of current capacity generated by reduction of ON resistance is enabled while a high withstand voltage is ensured, by relaxing the trade-off relation of an ON resistance and a withstand voltage, and its manufacturing method which can simply manufacture the element with excellent productivity.
SOLUTION: A semiconductor substrate region 32 which makes a current flow in the state of ON and is turned into **depletion** in the state of OFF is provided with n-buried regions 32b and p-buried regions 32c which are almost periodically and alternately formed in a plurality of depths. The n-buried regions 32b and the p-buried regions 32c are almost aligned in the depth direction. In the manufacturing method an n- high resistance layer 32a laminated by an epitaxial method and the n-buried regions 32b and the p-buried regions 32c are formed by diffusion of impurities.
COPYRIGHT: (C)2000,JPO

L58 ANSWER 10 OF 10 JAPIO COPYRIGHT 2002 JPO
AN 2001-015448 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN TAKEDA TORU; TSUNODA TETSUJIRO
PA TOSHIBA CORP
PI JP 2001015448 A 20010119 Heisei
AI JP1999-181687 (JP11181687 Heisei) 19990628
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
IC ICM H01L021-265
ICS H01L021-261 ; H01L021-266
AB PROBLEM TO BE SOLVED: To manufacture a low-loss power semiconductor device provided with a **super junction** which can be manufactured easily and is suitable for mass production, by controlling the acceleration energy of impurity ions and the area of the emitting area of the impurity ions.
SOLUTION: At the time of forming a striped P+ boron-implanted area 3a having a uniform width from the front surface to the rear surface of an N+ silicon wafer 1, it is necessary to form a uniform vertical boron distribution by continuously changing the acceleration energy of implanted boron ions and the range of boron in the wafer 1. Since the **lateral** extent of the implanted boron becomes broader as the range becomes longer, the concentration and width of the area 3a are made uniform in the vertical direction by controlling the width of the boron ion emitting area, so that the area becomes narrower as the acceleration energy becomes higher and the range of boron becomes longer.

L115 ANSWER 14 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 1995-171644 [23] WPIX
DNN N1995-134527
TI High voltage source electrode for LDMOST - is surrounded by separation region and has channel between source region and edge of back gate region and breakdown zones between drain and gate.
DC U12
IN LUDIKHUIZE, A W
PA (PHIG) PHILIPS ELECTRONICS NV; (PHIG) US PHILIPS CORP
CYC 8
PI EP 649177 A1 19950419 (199523)* EN 11p H01L029-78
R: DE FR GB IT NL
JP 07176744 A 19950714 (199537) 9p H01L029-78
BE 1007657 A3 19950905 (199542) NL 21p H01L000-00
US 5610432 A 19970311 (199716) 9p H01L023-58
EP 649177 B1 19980304 (199813) EN 12p H01L029-78
R: DE FR GB IT NL
DE 69408772 E 19980409 (199820) H01L029-78
AB EP 649177 A UPAB: 19950619
The semiconductor **RESURF** device has a **low-side** lateral DMOST (LDMOST). The device has a semiconductor body of predominantly one conductivity type and a surface area adjoining a surface of an opposite type. The LDMOST has a back gate region (5) in the surface region and a source region (6) of opposite types. A channel region (7) is defined between the source and the edge of the back gate region.

A drain (8) is near the back gate region and a separation region (15) of two levels of doping lies around the device. Several breakdown voltage raising zones (9) lie between drain and gate.

ADVANTAGE - Provides a **low-side** LDMOST with little or no increase in its ON-resistance during **switching** on and no leakage current.

Dwg.1/3
ABEQ US 5610432 A UPAB: 19970417
A semiconductor device of the **RESURF** type with a **low-side** lateral DMOST (LDMOST), comprising a semiconductor body of predominantly a first conductivity type and a surface region which adjoins a surface, which is of a second conductivity type opposed to the first, and which forms a first p-n **junction** with the semiconductor body at a **side** facing away from the surface, which LDMOST comprises a back gate region in the form of a surface zone of the first conductivity type provided in the surface region, with a source region in the form of a surface zone of the second conductivity type in the back gate region, and a channel region defined between the source region and an edge of the back gate region, and a drain region in the form of a surface zone of the second conductivity type situated at a distance from the back gate region, while a separation region of the first conductivity type is provided in the surface region around the LDMOST so as to adjoin the surface and extend towards the semiconductor body, and at least one first breakdown voltage raising zone of the first conductivity type is provided between the drain region and the back gate region and between the drain region and the separation region, which first breakdown voltage raising zone adjoins the surface, this surface being provided with an insulating layer on which a conductor track is provided which is connected to the drain region and which extends over at least one second voltage raising zone and the separation region, characterized in that at least one of the following zones: the zone forming the back gate region and the first breakdown voltage raising zone situated between the back gate and drain regions and situated most closely to the back gate region, is provided with at least one portion projecting towards the other zone at the area of which the distance between the two zones is smaller than in an adjoining portion of these zones, while the first breakdown voltage raising zone has no connection to said at least one second breakdown voltage raising zone over

which the conductor track extends, each of said first and second breakdown voltage raising zones separating said drain region from said back gate region.
Dwg.1/3

ADEQ EP 649177 B UPAB: 19980330

The semiconductor **RESURF** device has a **low-side** lateral DMOST (LDMOST). The device has a semiconductor body of predominantly one conductivity type and a surface area adjoining a surface of an opposite type. The LDMOST has a back gate region (5) in the surface region and a source region (6) of opposite types. A channel region (7) is defined between the source and the edge of the back gate region.

A drain (8) is near the back gate region and a separation region (15) of two levels of doping lies around the device. Several breakdown voltage raising zones (9) lie between drain and gate.

ADVANTAGE - Provides a **low-side** LDMOST with little or no increase in its ON-resistance during **switching** on and no leakage current.
Dwg.1/3

FS EPI

L115 ANSWER 13 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 1995-346351 [45] WPIX
DNN N1995-258972 DNC C1995-152121
TI Extended drain **resurf** lateral DMOS devices - comprises providing high voltage MOS device **lightly doped** drift region, and implanting addn. impurity concn., min. high voltage PMOS transistor.
DC L03 U11 U12
IN MALHI, S; MEI, C P
PA (TEXI) TEXAS INSTR INC
CYC 8
PI EP 676799 A2 19951011 (199545)* EN 16p H01L021-336
R: DE FR GB IT NL
JP 07297294 A 19951110 (199603) 20p H01L021-8234
US 5512495 A 19960430 (199623) 11p H01L021-336
EP 676799 A3 19960612 (199632) H01L021-336
TW 305057 A 19970511 (199733) H01L021-22
EP 676799 B1 20011205 (200203) EN H01L021-336
R: DE FR GB IT NL
DE 69524276 E 20020117 (200213) H01L021-336
AB EP 676799 A UPAB: 19951114
A method for making a high voltage Metal Oxide Semiconductor, MOS, device, comprises (1) providing a high voltage MOS device having a **lightly doped** drift region adjacent to a channel region, and (2) implanting an addn. impurity concn. in a rim of the drift region adjacent to the channel region.

Also claimed is a high voltage P-channel Metal Oxide Semiconductor, PMOS, device comprising:- (a) a high voltage drift region p-tank having a rim and a depth and having an impurity concn. of boron formed in a semiconductor substrate, (b) an n-type channel region adjacent to the rim of the drift region P-tank, (c) a high voltage field oxide having a thickness formed over a portion of the high voltage drift region, (d) a high voltage gate oxide formed over the channel region and having an edge overlying a portion of the high voltage field oxide, and (e) a **lateral junction** between the rim of the drift region p-tank and the channel region.

ADVANTAGE - The on-resistance of the high voltage PMOS transistor is minimised.

Dwg.0/3
ABEQ US 5512495 A UPAB: 19960610
A method for making a HV P-channel Metal Oxide Semiconductor, PMOS, device, comprising the steps of:

forming a **lightly doped** HV drift region p-tank having a p-type impurity concentration, the drift region being adjacent to an n-type channel region;

forming a vertical PN junction in a portion of the drift region p-tank which is adjacent to the n-type channel region by impurity segregation resulting from the growth of a HV field oxide; and

forming a horizontal PN junction between the drift region and the channel region by implanting a drift region rim adjustment in a portion of the drift region adjacent to the channel region and under a portion of the field oxide such that the vertical PN junction is cutoff and isolated from the channel region.

Dwg.0/3
FS CPI EPI

L58 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:450058 HCAPLUS
TI High voltage vertical conduction **superjunction** semiconductor device
IN Kinzer, Daniel M.; Sridevan, Srikant
PA International Rectifier Corporation, USA
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01L029-78
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002047171	A1	20020613	WO 2001-US47275	20011203
PRAI	US 2000-732401	A	20001207		

AB A high voltage vertical conduction semiconductor device has a plurality of deep trenches or holes in a lightly doped body of 1 cond. type. A diffusion of the other cond. type is formed in the trench walls to a depth and a concn. which matches that of the body so that, under reverse blocking, both regions fully deplete. The elongated trench or hole is filled with a dielec. which may be a composite of nitride and oxide layers having a **lateral** dimension change matched to that of the Si. The filler may be a highly resistive semi-insulating poly-Si which permits leakage current flow from source to drain to ensure a uniform elec. field distribution along the length of the trench during blocking.

L58 ANSWER 3 OF 10 INSPEC COPYRIGHT 2002 IEE DUPLICATE 1
AN 2002:7145826 INSPEC DN B2002-02-2560R-051
TI Poly flanked VDMOS (PFVDMOS): a superior technology for **superjunction** devices.
AU Gan, K.P.; Liang, Y.C.; Samudra, G.S. (Dept. of Electr. & Comput. Eng., Nat. Univ. of Singapore, Singapore); Xu, S.M.; Liu Yong
SO 2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)
Piscataway, NJ, USA: IEEE, 2001. p.2156-9 vol. 4 of 4 vol. (xxxiv+2228) pp. 11 refs.
Conference: Vancouver, BC, Canada, 17-21 June 2001
Price: CCCC 0-7803-7067-8/01/$10.00
ISBN: 0-7803-7067-8
DT Conference Article
TC New Development; Practical
CY United States
LA English
AB A novel VDMOS structure, named poly flanked VDMOS (PFVDMOS), is proposed for the first time to provide a better performance and process technology for **superjunction** MOSFET devices. The structure contains a thin oxide barrier to eliminate the existing p-n **lateral** interdiffusion problem, thus both the n-epi and p poly column widths can be reduced to a minimum. This reduction in column width enables the device to have a much higher n-epi doping concentration. In a sense, it leads to an optimal reduction in on-state resistance compared to other existing structures for the same voltage rating.

L46 ANSWER 7 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 97:397808 SCISEARCH
GA The Genuine Article (R) Number: WZ747
TI **Lateral** insulated gate bipolar transistor (LIGBT) structure based on partial isolation SOI technology
AU Udrea F (Reprint); Milne W; Popescu A
CS UNIV CAMBRIDGE, DEPT ENGN, CAMBRIDGE CB2 1PZ, ENGLAND (Reprint)
CYA ENGLAND
SO ELECTRONICS LETTERS, (8 MAY 1997) Vol. 33, No. 10, pp. 907-909.
Publisher: IEE-INST ELEC ENG, MICHAEL FARADAY HOUSE SIX HILLS WAY STEVENAGE, HERTFORD, ENGLAND SG1 2AY.
ISSN: 0013-5194.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 5
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB A new LIGBT structure based on partial isolation SOI technology is proposed and demonstrated through numerical simulations. In comparison with conventional SOI LIGBTs, the new structure offers an enhanced RESURF (**REduced SURface Field**) effect and improved heat dissipation with no compromise in the switching speed and on-stale resistance.
ST Author Keywords: silicon-on-insulator; insulated gate bipolar transistors

L115 ANSWER 17 OF 22 JAPIO COPYRIGHT 2002 JPO
AN 2001-135819 JAPIO
TI **SUPER-JUNCTION** SEMICONDUCTOR ELEMENT
IN UENO KATSUNORI
PA FUJI ELECTRIC CO LTD
PI JP 2001135819 A 20010518 Heisei
AI JP2000-189590 (JP2000189590 Heisei) 20000623
PRAI JP 1999-235174 19990823
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
IC ICM H01L029-78
ICS H01L029-861
AB PROBLEM TO BE SOLVED: To provide a **super-junction** semiconductor element which prevents generation of electric field convergence and realizes a high breakdown voltage in the **super-junction** semiconductor element comprising a parallel pn layer in which a current flows in an on state and which **depletes** in an off state.
SOLUTION: (1) A parallel pn layer of (n) drift regions 12d, 12f, 12h, 12j, 12l, and (p) partition regions 12c, 12e, 12g, 12i, 12k, 12m is provided outside an active region. (2) A first FP electrode 17a is provided on the (n) drift region 12d of the parallel pn layer outside the active region via an insulation film 19. The first FP electrode 17a comes into contact with a surface of the inside (p) partition region 12c, or is floated. It may by across a plurality of the (n) drift regions. Furthermore, a resistor is provided between the neighboring FP electrodes. (3) There is provided an (n) stopper region which reaches a low resistance layer outside the active region in a vertical direction of the parallel pn layer.

L58 ANSWER 8 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:523216 HCAPLUS
DN 121:123216
TI High-performance MESFET with multiple quantum wells
IN Mohammad, S. Noor; Renbeck, Robert B.
PA International Business Machines Corp., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L027-12
ICS H01L029-161; H01L045-00
NCL 257019000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5323020	A	19940621	US 1992-995459	19921222
	JP 07211891	A2	19950811	JP 1993-260052	19931018
	JP 2504376	B2	19960605		
	EP 607729	A2	19940727	EP 1993-480207	19931203
	R: DE, FR, GB				
	US 5420059	A	19950530	US 1994-198938	19940218
PRAI	US 1992-995459		19921222		

AB A **superheterojunction** FET contains a multiregion channel on a Si substrate. The device is a metal-semiconductor or junction FET. The multiregion channel has a 1st region of Si extending from the FET's source to a point under the FET's gate, beyond the gate's midpoint; a 2nd region extending from the first region to the FET's drain, comprised of a superlattice of alternating Si and SiGe layers; and a 3rd region of Si extending under the 1st two regions from the source to the drain. The first region has a **laterally** graded dopant that creates an accelerating elec. field. The superlattice structure increases electron mobility and transit velocity.

L58 ANSWER 9 OF 10 JAPIO COPYRIGHT 2002 JPO
AN 2002-009083 JAPIO
TI METHOD FOR FORMING REPETITIVE pn JUNCTION AND SEMICONDUCTOR DEVICE USING IT
IN HATSUTORI YOSHIKUNI; SUZUKI TAKASHI
PA TOYOTA CENTRAL RES & DEV LAB INC
PI JP 2002009083 A 20020111 Heisei
AI JP2000-190876 (JP2000190876 Heisei) 20000626
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
IC ICM H01L021-329
ICS H01L021-331 ; H01L029-73 ; H01L029-78 ; H01L021-336 ; H01L029-861
AB PROBLEM TO BE SOLVED: To provide a method for forming a repetitive pn junction having a low ON resistance and excellent breakdown strength characteristics, and a semiconductor device using that method.
SOLUTION: A p-type epitaxial layer 11 is formed on a p-type silicon substrate 10, and an n-type epitaxial layer 21 is formed on an n-type silicon substrate 20. Meanders 22a, 21a are then formed on respective substrates using RIE technology. Subsequently, the meanders 22a, 21a are fitted to each other and caused to react in high temperature atmosphere (mixture gas). Since a p-type film or an n-type film is formed in the gaps at the time of fitting, a more rigid and electrically stable repetitive pn junction is formed. Finally, it is polished from one substrate **side** to form a **super junction**. Since the p-layer and the n-layer are formed by epitaxial growth technology, a heavily doped pn junction is formed with high accuracy. According to the method a semiconductor device having a low ON resistance and a high withstand voltage can be fabricated.

L46 ANSWER 6 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 1998:295761 SCISEARCH
GA The Genuine Article (R) Number: ZG470
TI Integration of 5-V CMOS and high-voltage devices for display driver applications
AU Kim J D (Reprint); Park M Y; Kang J Y; Lee S Y; Koo J G; Nam K S
CS ETRI, SEMICOND TECHNOL DIV, UNIT PROC DEV SECT, TAEJON, SOUTH KOREA (Reprint)
CYA SOUTH KOREA
SO ETRI JOURNAL, (MAR 1998) Vol. 20, No. 1, pp. 37-45.
Publisher: ELECTRONICS TELECOMMUNICATIONS RESEARCH INST, 161 KAJONG-DONG, YUSONG-GU, TAEJON 305-350, SOUTH KOREA.
ISSN: 1225-6463.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 9
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB **Reduced surface field lateral** double-diffused MOS transistors for the driving circuits of plasma display panel and field emission display in the 120 V region have been integrated for the first time into a low-voltage 1.2 mu m analog CMOS process using p-type bulk silicon. This method of integration provides an excellent way of achieving both high power and low voltage functions on the same chip; it reduces the number of mask layers and also the cost of fabrication. The **lateral** double-diffused MOS transistor with a drift length of 6.0 mu m and a breakdown voltage greater than 150 V was self-isolated to the low voltage CMOS ICs. The measured specific on-resistance of the **lateral** double-diffused MOS is 4.8 m Omega.cm(2) at a gate voltage of 5 V.

L46 ANSWER 5 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 1998:788844 SCISEARCH
GA The Genuine Article (R) Number: 126HH
TI p-channel LDMOS transistor using new tapered field oxidation technology
AU Kim J (Reprint); Kim S G; Koo J G; Kim D Y
CS ELECT & TELECOMMUN RES INST, MICRO ELECT LAB TECHNOL, YUSONG POB 106, TAEJON 305600, SOUTH KOREA (Reprint)
CYA SOUTH KOREA
SO ELECTRONICS LETTERS, (17 SEP 1998) Vol. 34, No. 19, pp. 1893-1894.
Publisher: IEE-INST ELEC ENG, MICHAEL FARADAY HOUSE SIX HILLS WAY STEVENAGE, HERTFORD SG1 2AY, ENGLAND.
ISSN: 0013-5194.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 5
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB The on-resistance of p-channel RESURF (**reduced surface field**) LDMOS (**lateral** double-diffused MOS) transistors has been improved by using a new tapered TEOS field oxide in the drift region of the devices. With similar breakdown voltage, at V-gs = -5.0V, the specific on-resistance of the LDMOS with tapered field oxide is similar to 31.5m Omega . cm(2), while that of the LDMOS with conventional field oxide is similar to 57m Omega . cm(2).

L46 ANSWER 4 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 1998:930630 SCISEARCH
GA The Genuine Article (R) Number: 144HR
TI A new 800 V RESURF LDMOSFET with high SOA performance by using double-diffused drift region
AU Jin J H (Reprint); Kwon O K
CS HANYANG UNIV, DEPT ELECT ENGN, SEOUL 133791, SOUTH KOREA (Reprint)
CYA SOUTH KOREA
SO JOURNAL OF THE KOREAN PHYSICAL SOCIETY, (NOV 1998) Vol. 33, Supp. [S], pp. S212-S215.
Publisher: KOREAN PHYSICAL SOC, 635-4, YUKSAM-DONG, KANGNAM-KU, SEOUL 135-703, SOUTH KOREA.
ISSN: 0374-4884.
DT Article; Journal
FS PHYS
LA English
REC Reference Count: 11
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS

AB We propose anew **Reduced SURface Field** (RESURF) **Lateral** Double-diffused MOS (LDMOS) transistor structure with double-diffused drift region to enhance the Safe Operation Area (SOA) performance. In the proposed LDMOS transistor, another ion implantation step is added around the drain region after the n-drift drive-in to reduce the electric field and current crowding effect around the drain region. This results in the enhancement of the second breakdown voltage. Simulation results indicate that the proposed device has the specific on-resistance of 244 m Omega . cm(2) and the breakdown voltage of 790 V and the second breakdown voltage of the proposed device structure was enhanced from 300 V to 500 V in a conventional structure when Vgs=9 V. This is the best reported result in the 800 V class LDMOS devices.

L46 ANSWER 3 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 1999:673529 SCISEARCH
GA The Genuine Article (R) Number: 230GB
TI Improvement on P-channel SOI LDMOS transistor by adapting a new tapered oxide technique
AU Kim J (Reprint); Kim S G; Song Q S; Lee S Y; Koo J G; Ma D S
CS ELECT & TELECOMMUN RES INST, MICROELECT TECHNOL LAB, TAEJON 305600, SOUTH KOREA (Reprint); WOO SONG UNIV, DEPT ELECT & COMP ENGN, TAEJON 305718, SOUTH KOREA
CYA SOUTH KOREA
SO IEEE TRANSACTIONS ON ELECTRON DEVICES, (SEP 1999) Vol. 46, No. 9, pp. 1890-1894.
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394.
ISSN: 0018-9383.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 14
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB On-resistance of P-channel **REduced SURface Field** (RESURF) **lateral** double-diffused MOS (LDMOS) transistors has been improved by using a new tapered TEOS held oxide on the drift region of the devices, The nem tapered oxidation technique provides better uniformity, less than 3%, and reproducibility. With the similar breakdown voltage (V-B), at V-gs = -5.0 V, the specific on-resistance (R-sp) of the LDMOS with the tapered held oxide is about 31.5 m Omega.cm(2), while that of the LDMOS with the conventional field oxide is about R-sp = 57 m Omega.cm(2). The uniformities of R-sp and V-B are less than 5 and 3%, respectively.

L46 ANSWER 2 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2001:22383 SCISEARCH
GA The Genuine Article (R) Number: 383WX
TI High-voltage SOI power IC technology with non-RESURF n-LDMOSFET and RESURF p-LDMOSFET for PDP scan-driver applications
AU Roh T M (Reprint); Lee D W; Kim J; Kim S G; Song Q S; Kang J Y; Koo J G; Nam K S; Cho K I
CS Elect & Telecommun Res Inst, Microelect Technol Lab, Taejon 305350, South Korea (Reprint)
CYA South Korea
SO JOURNAL OF THE KOREAN PHYSICAL SOCIETY, (DEC 2000) Vol. 37, No. 6, pp. 889-892.
Publisher: KOREAN PHYSICAL SOC, 635-4, YUKSAM-DONG, KANGNAM-KU, SEOUL 135-703, SOUTH KOREA.
ISSN: 0374-4884.
DT Article; Journal
LA English
REC Reference Count: 10
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB A new power IC technology integrating non-**Reduced-SURface Field** (non-RESURF) n-channel **lateral** double-diffused MOSFET (n-LDMOSFET) and RESURF p-LDMOSFET into a 1.2 mum CMOS on a single chip was developed to apply to PDP scan-driver ICs. The developed power IC technique can reduce production cost and increase the process margin compared with conventional technique. The breakdown voltages of n- and p-LDMOSFETs were larger than 250 V, and their specific on-resistances were 50 m Omega . cm(2) and 140 m Omega . cm(2) respectively The PDP scan-driver IC fabricated by the proposed power IC technology showed good operation up to 250 V. The rising and the falling times of the PDP scan-driver IC were less than 110 nsec under Vdd=200 V and C-L=100 pF.

L46 ANSWER 1 OF 7 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2002:457388 SCISEARCH
GA The Genuine Article (R) Number: 555XY
TI Experimental and theoretical analysis of energy capability of RESURF LDMOSFETs and its correlation with static electrical safe operating area (SOA)
AU Khemka V (Reprint); Parthasarathy V; Zhu R H; Bose A; Roggenbauer T
CS Motorola Inc, Semicond Prod Sector, SmartMOS Technol Ctr, Mesa, AZ 85202 USA (Reprint)
CYA USA
SO IEEE TRANSACTIONS ON ELECTRON DEVICES, (JUN 2002) Vol. 49, No. 6, pp. 1049-1058.
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA.
ISSN: 0018-9383.
DT Article; Journal
LA English
REC Reference Count: 19
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB Thermal and electrical destruction of 55 V single and double **reduced surface field** (RESURF) **lateral** double-diffused MOSFETs (LDMOSFETs) in smart power ICs are investigated by experiments, simulations, and theoretical modeling. Static safe operating area (SOA) and single pulse dynamic SOA (energy capability) have been studied and correlated. Single RESURF device failure and hence the energy capability is controlled by electrical phenomenon for drain to source voltage near breakdown voltages. Whereas, the energy capability of the double RESURF device is shown to be controlled by thermal phenomenon for voltage ranges up to about 5 V below the breakdown voltage. Measured energy capability data have been used to obtain critical temperatures for device failure, which decreases with an increase in drain to source voltage. We have empirically shown using experimental data that if the dynamic SOA of the device comes within about 2-5X of the static SOA boundary, the device failure is strongly influenced by avalanche multiplication. An analytical model based on Green's function formulation is derived and proposed which can predict energy capability of LDMOSFETs for a wide range of device geometry. The calculated data show excellent matching with the measurements and are within +/-10%. A new technique of distributing power within a device by applying less power at the center and more at the edges is proposed, which realizes significant improvement in energy capability by optimizing the temperature distribution within the device.
ST Author Keywords: breakdown voltage; double RESURF; electrical failure; electrothermal; electrothermal failure; energy capability; intrinsic temperature; LDMOS; RESURF; safe operating area; single RESURF; smart power; specific on-resistance; SOA; thermal failure

L40 ANSWER 3 OF 3 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 1999:421533 SCISEARCH
GA The Genuine Article (R) Number: 200GZ
TI Analytical model for the electric field distribution in SOI **RESURF** and TMBS structures
AU Merchant S (Reprint)
CS MOTOROLA INC, SEMICOND PROD SECTOR, MESA, AZ 85202 (Reprint)
CYA USA
SO IEEE TRANSACTIONS ON ELECTRON DEVICES, (JUN 1999) Vol. 46, No. 6, pp. 1264-1267.
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394.
ISSN: 0018-9383.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 8
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB A simple analytical model for the electric field distribution in silicon-on-insulator (SOI) reduced surface field (**RESURF**) structures is developed. The model applies for uniform and linearly graded doping profiles. It is also applicable to **trench MOS** barrier Schottky (TMBS) rectifiers, which have a similar structure. The results are valuable for breakdown voltage, tunneling, hot carrier, and other electric field dependent analyses.

L44 ANSWER 1 OF 1 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 91:488903 SCISEARCH
GA The Genuine Article (R) Number: GC920
TI SIMULATION OF REVERSE BREAKDOWN IN PLANAR P-N-**JUNCTIONS**
AU HUANG Q (Reprint); AMARATUNGA G A J; NARAYANAN E M S; MILNE W I
CS UNIV CAMBRIDGE, DEPT ENGN, CAMBRIDGE CB2 1PZ, ENGLAND (Reprint)
CYA ENGLAND
SO SOLID-STATE ELECTRONICS, (1991) Vol. 34, No. 9, pp. 983-993.
DT Article; Journal
FS PHYS; ENGI
LA ENGLISH
REC Reference Count: 16
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS

AB The two-dimensional numerical simulator BAMBI has been modified to simulate reverse biased P-N **junction** characteristics. Complete I-V characteristics of the reverse biased P-N **junction** is obtained to predict the breakdown voltage rather than the ionization integral. Simulations are then applied to the field limiting ring (FLR) structure and the **reduced surface field** (RESURF) structure. A quasi-three-dimensional approach is used to simulate cylindrically symmetric P-N **junctions** to model the three-dimensional effects due to lateral curvature at corners of mask patterns. A resistive contact to the FLR is used to stabilize the numerical solution of floating FLRs. Simulation results suggest that the breakdown voltage of devices with smaller radii at the rounded corner are much lower as compared to predictions from two-dimensional simulation. In the case of the FLR and RESURF structures, three-dimensional effects play an important role in determining optimal design parameters.

L40 ANSWER 2 OF 3 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2001:506942 SCISEARCH
GA The Genuine Article (R) Number: 443DJ
TI Numerical analysis on the LDMOS with a double epi-layer and **trench** electrodes
AU Park I Y (Reprint); Choi Y I; Chung S K; Lim H J; Mo S I; Choi J S; Han M K
CS Elect & Telecommun Res Inst, Microelect Technol Lab, 161 Kajong Dong, Taejon 305600, South Korea (Reprint); Ajou Univ, Dept Mol Sci & Technol, Suwon 442749, South Korea; Ajou Univ, Dept Elect Engn, Suwon 442749, South Korea; Daewoo Elect, Div Semicond, Seoul, South Korea; Seoul Natl Univ, Sch Elect Engn, Seoul 151, South Korea
CYA South Korea
SO MICROELECTRONICS JOURNAL, (MAY-JUN 2001) Vol. 32, No. 5-6, pp. 497-502. Publisher: ELSEVIER ADVANCED TECHNOLOGY, OXFORD FULFILLMENT CENTRE THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, OXON, ENGLAND. ISSN: 0026-2692.
DT Article; Journal
LA English
REC Reference Count: 7
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB We proposed a new lateral double-diffused **MOS** (LDMOS) structure employing a double p/n epitaxial layer, which is formed on p(-) substrates. Trenched gate and drain are also employed to obtain uniform and high drift current density. The breakdown voltage and the specific on-resistance of the proposed LDMOS are numerically calculated by using a two-dimensional (2D) device simulator, MEDICI. The n(-) drift region and upper p(-) region of the proposed LDMOS are fully depleted in off-states employing the **RESURF** technique. The simulation results show that the breakdown voltage is 142 V and specific on-resistance is 183 m Omega mm(2) when the cell pitch of the LDMOS is 7.5 mum. The proposed LDMOS shows better trade-off characteristics than the previous results.

L40 ANSWER 1 OF 3 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2002:38539 SCISEARCH
GA The Genuine Article (R) Number: 506KC
TI Enhancement of breakdown voltage for SOI **RESURF** LDMOS employing a buried air structure
AU Kim S H (Reprint); Park I Y; Choi Y I; Chung S K
CS Ajou Univ, Dept Mol Sci & Technol, Suwon 442749, South Korea (Reprint); Elect & Telecommun Res Inst, Adv Microelect Res Lab, Taejon 305600, South Korea; Ajou Univ, Sch'Elect Engn, Suwon 442749, South Korea
CYA South Korea
SO JOURNAL OF THE KOREAN PHYSICAL SOCIETY, (DEC 2001) Vol. 39, Supp. [S], pp. S39-S41.
Publisher: KOREAN PHYSICAL SOC, 635-4, YUKSAM-DONG, KANGNAM-KU, SEOUL 135-703, SOUTH KOREA.
ISSN: 0374-4884.
DT Article; Journal
LA English
REC Reference Count: 10
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB An SOI **RESURF** LDMOS with the air as a buried insulator is proposed to increase the breakdown voltage. The air insulator call be formed by using **trench** and wet etching. The breakdown voltage characteristics are investigated by using two-dimensional device simulator, MEDICI. Simulated breakdown voltage of the proposed LDMOS is 54 % higher than that of the conventional LDMOS.

L50 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:531708 HCAPLUS
DN 133:113720
TI Fabrication of FET for increasing threshold voltage of corner device
IN Brown, Jeffrey S.; Gauthier, Robert J.; Voldman, Steven H.
PA International Business Machines Corporation, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-76
ICS H01L029-00
NCL 257374000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6097069	A	20000801	US 1998-102196	19980622
	TW 426991	B	20010321	TW 1999-88102073	19990210
	JP 2000269484	A2	20000929	JP 1999-159296	19990607
	JP 3207181	B2	20010910		
PRAI	US 1998-102196	A	19980622		

AB A structure for increasing the threshold voltage of a corner device, particularly for **shallow trench** isolation having narrow devices. An FET comprises a substrate having a channel formed therein under a gate between spaced source and drain regions. A trench isolation region is formed in the substrate around the transistor and on opposite sides of the channel to isolate the transistor from other devices formed in the substrate, with the trench isolation region forming first and second **junction** corner devices with opposite **sides** of the channel. A first dielec. layer is formed under the gate and over the channel of the field effect transistor to form a gate insulator for the transistor. A second corner edge dielec. layer is formed under the gate structure and over the first and second corner devices, such that the corner edge dielec. layer increases the thickness of dielec. over each corner device and thus increases the threshold voltage (Vt) and edge dielec. breakdown and decreases MOSFET corner gate-induced drain leakage.

L37 ANSWER 11 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2000:196261 SCISEARCH
GA The Genuine Article (R) Number: 290HV
TI SOI power devices
AU Udrea F (Reprint); Garner D; Sheng K; Popescu A; Lim H T; Milne W I
CS UNIV CAMBRIDGE, DEPT ENGN, ELECT ENGN DIV, TRUMPINGTON ST, CAMBRIDGE CB2 1PZ, ENGLAND (Reprint); UNIV CAMBRIDGE, DEPT ENGN, POWER DEVICES GRP, CAMBRIDGE CB2 1PZ, ENGLAND
CYA ENGLAND
SO ELECTRONICS & COMMUNICATION ENGINEERING JOURNAL, (FEB 2000) Vol. 12, No. 1, pp. 27-40.
Publisher: IEE-INST ELEC ENG, MICHAEL FARADAY HOUSE SIX HILLS WAY STEVENAGE, HERTFORD SG1 2AY, ENGLAND.
ISSN: 0954-0695.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 34
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB This paper provides an introduction to silicon-on-insulator (SOI) technology and the operating principles of high-voltage SOI devices, reviews the performance of the available SOI switching devices in comparison with standard silicon devices, discusses the reasoning behind the use of SOI technology in power applications and briefly covers the most advanced novel power SOI devices proposed to date. The impact of SOI technology in power integrated circuits (PICs) and the problems associated with the integration of high-voltage and low-voltage CMOS are also briefly analysed.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)	
FUJIHIRA T	1998		423	P ISPSD 98	<--

L115 ANSWER 20 OF 22 JAPIO COPYRIGHT 2002 JPO
AN 1992-074473 JAPIO
TI SEMICONDUCTOR DEVICE
IN YAMANISHI YUJI; TANIDA HIROSHI
PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
PI JP 04074473 A 19920309 Heisei
AI JP1990-189094 (JP02189094 Heisei) 19900716
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1224, Vol. 16, No. 291, P. 34 (19920626)
IC ICM (5) H01L029-784
AB PURPOSE: To use a source contact region of peripheral area as a **high-side switch** by making part of a gate side of the source contact region in P-type region with higher concentration than a P-type semiconductor substrate, and by not making the source contact region of the peripheral area in the punch-through preventive region.
CONSTITUTION: A N-channel MOSFET has a stripe structure in which a gate 6 of a source region 9 in peripheral area is put on the opposite side of a punch- through preventive region 10. An obliquely-lined portion 35 around the source region shows a **depletion** layer, when MOSFET is operating. In the peripheral area of a source 33, the source is located on the outside of a punch-through preventive region 36. Therefore, the **depletion** layer spreads in large area due to the low concentration of a semiconductor substrate 32. On the side of the gate, positive bias works in a gate electrode 34. As a result, the **depletion** layer also spreads in the area under the gate, and the yield on the gate **side** of **junction** between the source and the substrate does not occur.

L37 ANSWER 10 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2000:563752 SCISEARCH
GA The Genuine Article (R) Number: 336JG
TI A new generation of power MOSFET based on the concept of ''Floating Islands''
AU Cezac N (Reprint); Morancho F; Rossel P; Tranduc H; PeyreLavigne A
CS CNRS, LAAS, 7 AVE COLONEL ROCHE, F-31077 TOULOUSE 4, FRANCE (Reprint); MOTOROLA SEMICOND SA, F-31023 TOULOUSE, FRANCE
CYA FRANCE
SO EUROPEAN PHYSICAL JOURNAL-APPLIED PHYSICS, (JUN 2000) Vol. 10, No. 3, pp. 203-209.
Publisher: E D P SCIENCES, 7, AVE DU HOGGAR, PARC D ACTIVITES COURTABOEUF, BP 112, F-91944 LES ULIS CEDEXA, FRANCE.
ISSN: 1286-0042.
DT Article; Journal
FS PHYS
LA English
REC Reference Count: 10
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB In this paper, a new concept called ''Floating Islands diode'' (FLI-diode) is proposed: the voltage handling capability of this new diode is assumed by the association of several PN junctions in series. This concept can be applied to any power devices (lateral. or vertical). An example of vertical power MOSFET based on this concept is presented here: this new structure, called ''FLIMOSFET''', exhibits improved on-state resistance performance when compared to the conventional VDMOSFET. For instance, for a breakdown voltage of 900 volts, the theoretical performance are strongly improved in term of specific on-resistance (reduction of about 70% relative to the conventional structure and 40% relative to the silicon limit). Moreover the specific on-resistance theoretical limits of FLIMOSFET family are determined and compared to those of the ''Superjunction'' MOS Transistor family: this comparison shows the strong interest of the FLIMOSFET in the 200 volts-1000 volts breakdown voltage range.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)
FUJIHARA T	1998		423	P INT S POW SEM DEV <--

L37 ANSWER 9 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2000:746951 SCISEARCH
GA The Genuine Article (R) Number: 358RE
TI 120 V interdigitated-drain LDMOS (IDLDMOS) on SOI substrate breaking power LDMOS limit
AU Xu S M (Reprint); Gan K P; Samudra G S; Liang Y C; Sin J K O
CS VISHAY SILICONIX, SANTA CLARA, CA 95054 (Reprint); NATL UNIV SINGAPORE, DEPT ELECT & COMP ENGN, SINGAPORE 119260, SINGAPORE; HONG KONG UNIV SCI & TECHNOL, DEPT ELECT & ELECT ENGN, KOWLOON, HONG KONG, PEOPLES R CHINA
CYA USA; SINGAPORE; PEOPLES R CHINA
SO IEEE TRANSACTIONS ON ELECTRON DEVICES, (OCT 2000) Vol. 47, No. 10, pp. 1980-1985.
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394.
ISSN: 0018-9383.
DT Article; Journal
FS ENGI
LA English
REC Reference Count: 16
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS

AB A new device structure named IDLDMOS is proposed to overcome the power LDMOS limit (R-on, (sp) proportional to BVdss2.5). The concept is based on replacing LDMOS lightly doped n-drift region by moderately doped alternating p and n layers of suitable dimension and doping. Off state requirement is achieved by mutual lateral-depletion of the alternating layers, Using small identical lateral width for both p and n layers, a doping concentration of up to two orders of magnitude higher than n-drift concentration in a conventional case can be achieved to reduce the on-resistance R-on. The simulated 120 V IDLDMOS on SOI substrate has shown a R-on value that is about 38% of the corresponding R-on value of a conventional n(-) LDD type LDMOS, At a R-on, (sp) value of 1.15 m Omega-cm(2) with BVdss of 124 V, IDLDMOS has exceeded the conventional LDMOS limit. Compared to conventional LDMOS, IDLDMOS is less prone to quasisaturation at high gate and drain voltage due to its higher drain doping. Isothermal simulation has shown that there was no deterioration in both ac and transient performance between the two devices, Nevertheless, the lower V-d, (sat) of IDLDMOS is expected to yield a higher g(m), at the same level of current conduction as in the conventional structure.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)
FUJIHARA T	1998		423	P INT S POW SEM DEV <--

L37 ANSWER 8 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2000:831692 SCISEARCH
GA The Genuine Article (R) Number: 369KU
TI An analytical model for the 3D-RESURF effect
AU Ng R (Reprint); Udrea F; Amaratunga G
CS UNIV CAMBRIDGE, DEPT ENGN, CAMBRIDGE CB2 1PZ, ENGLAND (Reprint)
CYA ENGLAND
SO SOLID-STATE ELECTRONICS, (OCT 2000) Vol. 44, No. 10, pp. 1753-1764.
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND.
ISSN: 0038-1101.
DT Article; Journal
FS PHYS; ENGI
LA English
REC Reference Count: 21
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB This paper presents an analytical model for the determination of the basic breakdown properties of three-dimensional (3D)-RESURF/CoolMOS/super junction type structures. To account for the two-dimensional (2D) effect of the 3D-RESURF action. 2D models of the electric field distribution are developed. Based on these, expressions are derived for the breakdown voltage as a function of doping concentration and physical dimensions. In addition to cases where the drift regions are fully depleted, the model developed is also applicable to situations involving drift regions which are almost depleted. Accuracy of the analytical approach is verified by comparison with numerical results obtained from the MEDICI device simulator.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)	
FUJIHIRA T	1998		423	ISPSD	<--

L37 ANSWER 7 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2001:178539 SCISEARCH
GA The Genuine Article (R) Number: 402ZE
TI Optimization of the specific on-resistance of the COOLMOS (TM)
AU Chen X B (Reprint); Sin J K O
CS Univ Elect Sci & Technol China, Dept Elect Engn, Sichuan 610054, Peoples R China (Reprint); Hong Kong Univ Sci & Technol, Dept Elect & Elect Engn, Hong Kong, Hong Kong, Peoples R China
CYA Peoples R China
SO IEEE TRANSACTIONS ON ELECTRON DEVICES, (FEB 2001) Vol. 48, No. 2, pp. 344-348.
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA.
ISSN: 0018-9383.
DT Article; Journal
LA English
REC Reference Count: 14
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB The optimized values for the physical and geometrical parameters of the p- and n-regions used in the voltage-sustaining layer of the COOLMOS(TM)(1) are presented. Design of the parameters is aimed to produce the lowest specific on-resistance, R-on, for a given breakdown voltage, V-B. A new relationship between the R-on and V-B for the COOLMOS(TM) is developed as R-on = C.V-B(1.32), where the constant C is dependent on the cell dimension and pattern geometry. It is also found that by putting a thin layer of insulator between the p-region and its neighboring n-regions, the value of R-on can be further reduced. The possibility of incorporating the insulating layer may open up opportunities for practical implementation of the COOLMOS(TM) for volume production.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)	
FUJIHIRA T	1998		423	P ISPSD	<--

L37 ANSWER 6 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2001:195083 SCISEARCH
GA The Genuine Article (R) Number: 405FR
TI Theory of the switching response of CBMOST
AU Chen X B (Reprint)
CS Univ Elect Sci & Technol China, Res Inst Micro Elect, Chengdu 610054, Peoples R China (Reprint)
CYA Peoples R China
SO CHINESE JOURNAL OF ELECTRONICS, (JAN 2001) Vol. 10, No. 1, pp. 1-6. Publisher: TECHNOLOGY EXCHANGE LIMITED HONG KONG, 26-28 AU PUI WAN ST, STE 1102, FO TAN INDUSTRIAL CENTRE, FO TAN, SHATIN, HONG KONG. ISSN: 1022-4653.
DT Article; Journal
LA English
REC Reference Count: 11
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB A theory of the switching response of the CBMOST (or COOLMOST, or Super Junction device) is proposed based on the physical and geometrical parameters inherent in the voltage sustaining structure. It is proven that the salient feature of such a device is that the storage time in turn-off process is a little longer than the conventional power MOST due to its heavier doping, Explanation for the fast turn-on process despite of having an oppositely doped region inside the voltage sustaining layer is also given. It is also shown that if p- (or n-) regions in the CB-structure are not directly contacted to the n(+) (or p(+)) drain region, then the device is a normally-on one. Measures are proposed for the real device to be not normally-on.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)
FUJIHIRA T	1998		493	P 11 ISPID IEEE <--

L37 ANSWER 5 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2001:506941 SCISEARCH
GA The Genuine Article (R) Number: 443DJ
TI Power superjunction devices: an analytic model for breakdown voltage
AU Strollo A G M; Napoli E (Reprint)
CS Univ Naples Federico II, Dept Elect Engn, Via Claudio 21, I-80125 Naples, Italy (Reprint); Univ Naples Federico II, Dept Elect Engn, I-80125 Naples, Italy
CYA Italy
SO MICROELECTRONICS JOURNAL, (MAY-JUN 2001) Vol. 32, No. 5-6, pp. 491-496. Publisher: ELSEVIER ADVANCED TECHNOLOGY, OXFORD FULFILLMENT CENTRE THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, OXON, ENGLAND. ISSN: 0026-2692.
DT Article; Journal
LA English
REC Reference Count: 14
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB The paper presents an analytic two-dimensional (2D) model for breakdown voltage of recently proposed superjunction structures. The 2D model is able to correctly estimate electric field and breakdown voltage giving an insight into superjunction devices behavior.

Proposed closed form equations for superjunction dimensions and doping as a function of breakdown voltage are useful guidelines to optimal design. The 2D model overcomes the limits of 1D approximations that are likely to overestimate breakdown voltage. (C) 2001 Published by Elsevier Science Ltd. All rights reserved.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)	
FUJIHIRA T	1998		423	P ISPSD	<--

L37 ANSWER 4 OF 11 SCISEARCH COPYRIGHT 2002 ISI (R)
AN 2001:600352 SCISEARCH
GA The Genuine Article (R) Number: 455WN
TI Oxide-bypassed VDMOS (OBVDMOS): An alternative to superjunction high voltage MOS power devices
AU Liang Y C (Reprint); Gan K P; Samudra G S
CS Natl Univ Singapore, Dept Elect & Comp Engn, Singapore 119260, Singapore (Reprint)
CYA Singapore
SO IEEE ELECTRON DEVICE LETTERS, (AUG 2001) Vol. 22, No. 8, pp. 407-409.
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA.
ISSN: 0741-3106.
DT Article; Journal
LA English
REC Reference Count: 14
ABSTRACT IS AVAILABLE IN THE ALL AND IALL FORMATS
AB Superjunction concept had been proposed to overcome ideal silicon MOSFET limit, but its fabrication was handicapped by the precise charge balance requirement and inter-diffusion problem. We report a novel device structure termed oxide-bypassed VDMOS (OBVDMOS) that requires the well-established oxide thickness control instead of the difficult doping control in translating the limit to a higher blocking voltage, This is done by using metal-thick-oxide (MTO) at the sidewalls of drift region. One can choose to have a higher blocking voltage or increase the background doping. A PiN structure, essentially identical to MOSFET during off state, was fabricated to demonstrate the proposed concept, Its measured BVdss of 170 V is 2.5 times higher than measured conventional device BVdss of 67 V on the same silicon wafer.

Referenced Author (RAU)	Year (RPY)	VOL (RVL)	PG (RPG)	Referenced Work (RWK)	
FUJIHIRA T	1998		423	P ISPSD	<--

L30 ANSWER 2 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 2000-499389 [44] WPIX
DNN N2000-370138 DNC C2000-149941
TI Formation of extended drain of high voltage field effect transistor (HVFET) having low on-state resistance.
DC L03 U11 U12
IN AJIT, J S; DISNEY, D R; RUMENNIK, V
PA (POWE-N) POWER INTEGRATIONS INC
CYC 91
PI WO 2000046851 A1 20000810 (200044)* EN 45p H01L021-425
AU 2000029770 A 20000825 (200059) H01L021-425
US 6168983 B1 20010102 (200103) H01L021-337
EP 1163697 A1 20011219 (200206) EN H01L021-425
AB WO 200046851 A UPAB: 20000913
NOVELTY - The method comprises

(a) forming a well region (17) of a first conductivity type in a substrate of a second conductivity type, the well region having a **laterally** extended portion (23),

(b) implanting a dopant of the second conductivity type into the **laterally** extended portion of the well region to form a buried region (18), and

(c) forming a drain diffusion region (19) of the first conductivity type in the well.

DETAILED DESCRIPTION - Preferred features - The buried region is disposed beneath a surface of the substrate. Step (a) comprises implanting a dopant of the first conductivity type into the substrate, and diffusing the dopant into the substrate. The first conductivity type is n-type and the second conductivity type is p-type. The drain diffusion region is spaced-apart from the buried region. The buried region is sandwiched within the well region such that dual **junction** FET conduction channels are formed above and below the buried region.

USE - For the manufacture of HVFET structures that include an insulated gate FET in series with a **junction** FET.

ADVANTAGE - A minimal number of processing steps are required to form the parallel JFET conduction channels which provide the HVFET with a low on-state resistance.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the HVFET.

N-well region 17
Buried region 18
Drain diffusion region 19
Lateral boundary 21
Laterally extended drain portion 23
Dwg.1/14

L30 ANSWER 1 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 2000-601771 [57] WPIX
CR 1998-287310 [25]
DNN N2000-445314
TI High voltage field effect transistor includes multi layer conduction region.
DC U12
IN AJIT, J S; DISNEY, D R; RUMENNIK, V
PA (POWE-N) POWER INTEGRATIONS INC
CYC 91
PI WO 2000046859 A1 20000810 (200057)* EN 39p H01L029-76
AU 2000027467 A 20000825 (200059) H01L029-76
US 6207994 B1 20010327 (200119) H01L029-76
EP 1163700 A1 20011219 (200206) EN H01L029-76
US 2002050613 A1 20020502 (200234) H01L029-792
US 2002053698 A1 20020509 (200235) H01L031-119
AB WO 200046859 A UPAB: 20020528
NOVELTY - The transistor includes both a drain diffusion region and a source diffusion region of opposite conductivity types. Between the source diffusion region and the **lateral** boundary (21) is a channel region (28). Above is an insulated gate (between 27+16) to control current flow. Within the **laterally** extended portion of the first region is a buried region of the first conductivity. This forms a **junction** field-effect structure.

USE - For circuits requiring a high voltage transistor.

ADVANTAGE - The new transistor exhibits a low specific on state resistance and the required minimum breakdown voltage, in a small area. Also, it may be integrated readily onto a chip which includes low voltage logic devices, and is relatively inexpensive to manufacture.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic of the transistor.

Source diffusion region 10
Drain diffusion region 11
Channel region 28
Lateral boundary 21

Dwg.1/22

L28 ANSWER 11 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1997-536115 [49] WPIX
DNN N1997-446274
TI Doped region formation in semiconductor substrate - forming doped region in substrate by forming **trenches** filled with epitaxially grown doped semiconductor layer and by electrochemical etching.
DC U11 U12
IN GRUENING, U; LEHMANN, V; SCHAEFER, H; STENGL, R; WENDT, H
PA (SIEI) SIEMENS AG
CYC 20
PI WO 9740527 A1 19971030 (199749)* DE 18p H01L021-20
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP US
ADT WO 9740527 A1 WO 1997-DE707 19970407
PRAI **DE 1996-19615920 19960422**
REP 1.Jnl.Ref; DE 4340205; EP 296348; EP 390522; GB 2017401; JP 2111062; US 3740276; US 5216275; US 5438215
IC ICM H01L021-20
ICS H01L021-3063; H01L021-336; H01L029-06
AB WO 9740527 A UPAB: 19971211
A doped region is formed in a semiconductor substrate by forming **trenches** in the substrate. The **trenches** are filled with an epitaxially grown, doped semiconductor layer. The depth of the trench is greater than a linear deformation of the trench parallel to the main surface of the semiconductor substrate.

The flanks of the trench are tilted by 0.01 to 3 deg. w.r.t. the normal of the main surface which includes monocrystalline silicon. The **trenches** are formed by electrochemical etching in a fluoride-containing, acidic electrolyte in contact with the main surface. The epitaxy is carried out at 700 to 900 deg. C. at a pressure of 1 to 20 Torr.

USE/ADVANTAGE - Vertical doping of semiconductors, esp. for power MOSFETs with trench technology. Doped regions can be formed deep.
Dwg.2/3
FS EPI

L28 ANSWER 10 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1999-396228 [34] WPIX
DNN N1999-296237
TI Lateral high voltage transistor - has **trenches** in epitaxial layer in rows and columns between source and drain electrodes with walls doped with dopant of first conductive type.
DC U12
IN TIHANYI, J
PA (SIEI) SIEMENS AG
CYC 20
PI DE 19828191 C1 19990729 (199934)* 4p H01L029-78
WO 9967826 A1 19991229 (200008) DE H01L029-06
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
EP 1008184 A1 20000614 (200033) DE H01L029-06
R: DE FR GB IE IT
US 6326656 B1 20011204 (200203) H01L029-72
ADT DE 19828191 C1 DE 1998-19828191 19980624; WO 9967826 A1 WO 1999-DE761 19990317; EP 1008184 A1 EP 1999-913117 19990317, WO 1999-DE761 19990317; US 6326656 B1 Cont of WO 1999-DE761 19990317, US 2000-511813 20000224
FDT EP 1008184 A1 Based on WO 9967826
PRAI **DE 1998-19828191 19980624**
IC ICM H01L029-06; H01L029-72; H01L029-78
AB DE 19828191 C UPAB: 19990825
The lateral high voltage transistor has a semiconductor body (1,2). The semiconductor body has a weakly doped semiconductor substrate (1) of a first conductive type. An epitaxial layer (2) of the opposite conductive type is provided on the semiconductor substrate (1).

The transistor also has a drain electrode (3), a source electrode (5) and a gate electrode (7). A semiconductor zone (4) of the first conductive type is provided under the gate electrode (7) and is embedded in the epitaxial layer (2). **Trenches** (8) are provided in the epitaxial layer (2) arranged in rows and columns between the source electrode (5) and the drain electrode (3). The walls of the **trenches** (8) are highly doped with dopant of the first conductive type.

USE - Transistor is used for HV-FET. LIGBT.

ADVANTAGE - Transistor has structure which can be manufactured in relatively simple manner.

Dwg.1/2
FS EPI
FA AB; GI

L28 ANSWER 9 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2000-161384 [14] WPIX
DNN N2000-120385
TI MOSFET manufacture with pn junction trench sidewall structure by diffusion.
DC U11 U12
IN MINATO, T; NITTA, T; UENISI, A
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 24
PI WO 2000005767 A1 20000203 (200014)* JA 61p H01L029-78
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP KR US
EP 1026749 A1 20000809 (200039) EN H01L029-78
R: CH DE FR IT LI NL
TW 398070 A 20000711 (200106) H01L027-04
CN 1279822 A 20010110 (200128) H01L029-78
JP 11549150 X 20010424 (200130) H01L029-78
KR 2001024224 A 20010326 (200161) H01L029-78
US 6307246 B1 20011023 (200165) H01L023-58
AB WO 200005767 A UPAB: 20000320
NOVELTY - The device has **trenches** (5a) in a semiconductor substrate. P-type (2) and N-type (3) sidewall diffusion regions constitute a pn junction along the depthwise direction of the trench. A heavily doped n+ -type substrate region (1) is formed on the lower surface of the diffused region with a depth (Td) of the trench deeper than the depth (Nd) of p and n-type diffused region by at least a diffusion length (L).
USE - Formation of metal-oxide-semiconductor field-effect transistors (MOSFETs).
ADVANTAGE - The semiconductor device has a high breakdown strength and low ON resistance.
DESCRIPTION OF DRAWING(S) - The figure shows a section through the trench structure of the device.
n+ -type substrate region 1
P and N-type sidewall diffused regions 2,3
Trenches 5a
Diffusion length L
Diffusion depth Nd
n+ substrate trench depth Td
Dwg.1/45
FS EPI

L28 ANSWER 7 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2001-025057 [03] WPIX
DNN N2001-019519 DNC C2001-007718
TI Silicon carbide Schottky rectifier for switching in high power devices includes charge coupling region forming p-n junction with doped drift mesa.
DC L03 U12
IN BALIGA, B J
PA (UYNC-N) UNIV NORTH CAROLINA STATE
CYC 86
PI WO 2000070684 A2 20001123 (200103)* EN 47p H01L029-24
AU 2000048535 A 20001205 (200113) H01L029-24
US 6313482 B1 20011106 (200170) H01L031-0312
ADT WO 2000070684 A2 WO 2000-US13455 20000516; AU 2000048535 A AU 2000-48535 20000516; US 6313482 B1 US 1999-312980 19990517
FDT AU 2000048535 A Based on WO 200070684
PRAI **US 1999-312980 19990517**
IC ICM H01L029-24; H01L031-0312
ICS H01L029-06; H01L029-78; H01L029-808; H01L029-872
AB WO 200070684 A UPAB: 20010116
NOVELTY - Silicon carbide Schottky rectifier includes silicon carbide substrate with doped drift region (12) defined by two **trenches**. Charge coupling regions (14a,14b) doped with opposite type to drift regions are formed in the **trenches**. The charge coupling regions in the **trenches** form p-n rectifying junctions with the drift mesa. A Schottky rectifying contact is formed on the mesa.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a silicon carbide UMOSFET which has an insulated gate electrode in the trench. A semi-insulating region with resistivity of 10exp14-10exp18 ohm.cm is electrically connected to the drift region.

USE - The device is used for switching devices for high power applications.

ADVANTAGE - The switching device has low on-state resistance and high blocking voltage capability.

DESCRIPTION OF DRAWING(S) - The figure shows a cross section of the Schottky rectifier.
Drift region 12
Charge coupling regions 14a,14b
Dwg.2/15

L28 ANSWER 8 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2000-283719 [24] WPIX
DNN N2000-213492
TI Semiconductor component manufacturing method esp. for compensation components, such as transistors - involves forming intermediate interlocking zones of first and second conductivity type by doping out of **trenches** with subsequent filling.
DC U12
IN DEBOY, G; FRIZA, W; HAEBERLEN, O; RUEB, M; STRACK, H; HABERLEN, O; RUB, M
PA (SIEI) SIEMENS AG; (INFN) INFINEON TECHNOLOGIES AG; (DEBO-I) DEBOY G; (FRIZ-I) FRIZA W; (HABE-I) HABERLEN O; (RUBM-I) RUB M; (STRA-I) STRACK H
CYC 22
PI WO 2000017937 A2 20000330 (200024)* DE 45p H01L029-78
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
DE 19843959 A1 20000406 (200024) H01L021-334
EP 1110244 A1 20010627 (200137) DE H01L029-78
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 2001053568 A1 20011220 (200206) H01L021-332
KR 2001075354 A 20010809 (200211) H01L029-78
AB WO 200017937 A UPAB: 20020215
The method involves providing for a semiconductor component comprising a semiconductor body having a blocking pn-junction, a first zone (7) of a first conductivity type joined to a first electrode (10) and adjoining a zone (6) which forms the blocking pn-junction and which has a second conductivity type opposite to that of the first; a second zone (1) of the first conductivity type is connected to a second electrode. The side of zone (6) facing the second zone (10 forms a first surface (A), and in the region between the first (A) and second (B) surfaces are interlocking zones (4,5) of first and second conductivity types.

The zones (4) and (5) are formed by doping out of **trenches** (11,14) with subsequent filling, so that in the regions (I) near the first surface (A) charge carriers of the second conductivity type predominate and in regions (III) near the second surface (B) charge carriers of the first conductivity type predominate.

USE - For n-channel and p-channel MOSFETs, diodes, thyristors, GTOs etc.

ADVANTAGE - Enables manufacture of first and second conductivity type zones with required variable doping.

3,4a,16/16

L28 ANSWER 5 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2001-495735 [54] WPIX
DNN N2001-367277
TI Semiconductor device manufacture for automotive electronic system, involves filling **trenches** with p-doped polysilicon material cooperating with either of **trenches** to form active region and termination structure.
DC U11
IN ROBB, F Y; ROBB, S P; SHEN, Z
PA (SEMI-N) SEMICONDUCTOR COMPONENTS IND LLC
CYC 1
PI US 6204097 B1 20010320 (200154)* 6p H01L021-332
ADT US 6204097 B1 US 1999-259602 19990301
PRAI **US 1999-259602 19990301**
IC ICM H01L021-332
AB US 6204097 B UPAB: 20010924
NOVELTY - The exposed portion of oxide layer and drift layer (14) below the oxide layer are etched to form **trenches** (22,23). The p-doped polysilicon trench fill material (24) is formed in **trenches**. The material (24) cooperates with the trench (22) to form active region (21) and material (24) cooperates with the trench (23) to form termination structure (25').

DETAILED DESCRIPTION - The drift layer (14) is of n-type conductivity formed on buffer layer (13) on the substrate.

USE - For automotive electronics, portable electronics, power supplies and telecommunication.

ADVANTAGE - As the power semiconductor devices having a reduced on resistance is manufactured using fewer marking steps the manufacturing cost is lowered.

DESCRIPTION OF DRAWING(S) - The figure shows the enlarged cross-sectional view of semiconductor device.

Buffer layer 13
Drift layer 14
Active region 21
Trenches 22,23
Material 24
Termination structure 25'
Dwg.5/5

L11 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:335769 HCAPLUS
DN 132:328624
TI Semiconductor component and procedure for its production.
IN **Miyasaka, Yasushi**; Fujihira, Tatsuhiko; Ohnishi, Yasuhiko; Ueno, Katsunori; Iwamoto, Susumu
PA Fuji Electric Co., Ltd., Japan
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
IC ICM H01L029-06
ICS H01L029-78; H01L029-737; H01L021-336
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19954351	A1	20000518	DE 1999-19954351	19991111
	JP 2001111041	A2	20010420	JP 1999-237286	19990824
	US 6291856	B1	20010918	US 1999-438078	19991110
	US 2001046739	A1	20011129	US 2001-906557	20010716
PRAI	JP 1998-321567	A	19981112		
	JP 1999-221861	A	19990805		
	US 1999-438078	A3	19991110		

AB The invention describes the effects of parameters and makes the mass prodn. possible of a semiconductor component with **super** junctions, possessing a drift layer, consisting of a pn parallel layer, which in the ON state conducts electricity and is depleted in the OFF position. The dopant abundance in the n-drift zones lies in the range between 100% and 150% or between 110% and 150% of the quantity of dopant in the p-buffer zones. The dopant d.in any one zone-type, i.e. the drift zone or the buffer zone, lies in the range of 92% to 108% of the dopant d.in the other zone. In addn. the width for one zone-type lies within the range between 94% and 106% the width of the other zone-type.

L30 ANSWER 3 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1997-344410 [32] WPIX
CR 2001-302463 [32]; 2002-132550 [31]; 2002-132551 [31]; 2002-132552 [31]; 2002-132553 [31]; 2002-132554 [31]
DNC C1997-110763
TI Semiconductive device with **lateral** or vertical structure of drift regions - allows a reduction in the ON resistance in addition to an increase in breakdown voltage.
AW TRANSISTOR MOSFET DIODE THYRISTOR.
DC L03 U11 U12
IN FUJIHIRA, T
PA (FJIE) FUJI ELECTRIC CO LTD
CYC 4

PI	GB 2309336	A	19970723 (199732)*	75p	H01L029-66
	DE 19702102	A1	19970724 (199735)	30p	H01L029-78
	JP 09266311	A	19971007 (199750)	15p	H01L029-78
	US 6097063	A	20000801 (200039)		H01L029-94
	GB 2309336	B	20010523 (200130)		H01L029-66
	US 6294818	B1	20010925 (200158)		H01L029-76
	JP 2001352075	A	20011221 (200206)	17p	H01L029-786
	JP 2002083961	A	20020322 (200236)	14p	H01L029-78
	JP 2002100783	A	20020405 (200239)	14p	H01L029-861

AB GB 2309336 A UPAB: 20020621
A semiconductor device has a drift region (190) which flows a drift current if it is in an ON mode and is depleted if it is in an OFF mode. The drift region comprises first conductive type divided drift path regions (DPR) (1) which are parallel connected together. Positioned between adjacent DPR are second conductive type side regions (SR) (2) to form p-n **junctions**.

A method of manufacturing the semiconductor device is also claimed.

USE - For e.g. a metal-oxide field effect transistor (MOSFET), an IGBT, a thyristor, a HEMT, a bipolar transistor and semiconductor diode.

ADVANTAGE - The device relaxes the relationship between the ON resistance and the breakdown voltage. This enables an increase in the current capacity under high breakdown voltage.

Dwg.6a/12

L11 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:322398 HCAPLUS
TI Semiconductor component as well as procedure for the production of the same [Machine Translation].
IN Shindou, Youichi; **Miyasaka, Yasushi; Fujihira, Tatsuhiko**; Takei, Manabu
PA Fuji Electric Co., Ltd., Japan
SO Ger. Offen.
CODEN: GWXXBX
DT Patent
LA German
IC ICM H01L029-06
ICS H01L029-78; H01L029-737; H01L021-336
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19954352	A1	20000518	DE 1999-19954352	19991111
	JP 2001015752	A2	20010119	JP 1999-308523	19991029
PRAI	JP 1998-319672	A	19981111		
	JP 1999-121224	A	19990428		

AB [Machine Translation of Descriptors]. The invention obtains a semiconductor component with **superzone** transition, which exhibits a drift layer in form of a pn parallel layer, leads the electricity in the EIN condition and became impoverished in the AUS condition, whereby the element exhibits a high reverse voltage. One n-zone of high resistance is formed at the periphery of the drift layer, which consists of n-Driftzonen and p-Trennzonen. The dopant density of the zone of high resistance amounts to 5.62 x 1017 x VDSS -1,36 cm-3 less or. VDSS designates therein the withstand voltage in volts. A n-zone of low resistance is adjacent on n- the zone of high resistance intended.

L11 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:695846 HCAPLUS
DN 130:19365
TI Simulated **superior** performances of semiconductor **superjunction** devices
AU **Fujihira, Tatsuhiko; Miyasaka, Yasushi**
CS Matsumoto Factory, Fuji Electric Co., Ltd., Matsumoto, 390-0821, Japan
SO Proceedings of the International Symposium on Power Semiconductor Devices & ICs, 10th, Kyoto, June 3-6, 1998 (1998), 423-426 Publisher: Institute of Electrical Engineers of Japan, Tokyo, Japan.
CODEN: 66WCAU
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB Performances of majority- and minority-carrier semiconductor **superjunction** devices are examd. and compared to that of std. devices in terms of forward c.d., reverse leakage current, and switching charge. Based on two-dimensional simulations and theor. calcns., it is shown that two orders of magnitude improvement in forward c.d., an order of magnitude improvement in switching charge for majority-carrier **superjunction** devices, and an order of magnitude improvement in forward c.d. for minority-carrier **superjunction** devices are feasible when compared to std. devices.
ST semiconductor **superjunction** device performance electron carrier

L11 ANSWER 6 OF 6 JAPIO COPYRIGHT 2002 JPO
AN 2000-208527 JAPIO
TI MANUFACTURE OF **SUPER**-JOINT SEMICONDUCTOR ELEMENT AND THE **SUPER**-JOINT SEMICONDUCTOR ELEMENT
IN **MIYASAKA YASUSHI; FUJIHIRA TATSUHIKO**
PA FUJI ELECTRIC CO LTD
PI JP 2000208527 A 20000728 Heisei
AI JP1999-004176 (JP11004176 Heisei) 19990111
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
IC ICM H01L021-329
ICS H01L021-265 ; H01L029-78 ; H01L021-336 ; H01L029-861
AB PROBLEM TO BE SOLVED: To provide a manufacture which can manufacture with **superior** mass productivity and readily **super**-joint semiconductor elements, in which a trade-off relation between an on-resistance and a breakdown voltage is improved and an increase in current capacity due to reduction in on-resistance is possible, irrespective of a high breakdown voltage.
SOLUTION: In this manufacturing method, in an on-state, a current flows, and in an off-state, at least one of a depleting n drift region 22a and p partition region 22b, for example, the p partition region 22b is formed with ion implantation, in particular, ion implantation in which an accelerating voltage continuously changes. Another region may be formed by epitaxial growth, or may be formed by diffusion of surface emptiness.
COPYRIGHT: (C)2000,JPO

L22 ANSWER 7 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1989-285492 [39] WPIX
DNN N1989-217920 DNC C1989-126487
TI Integrated circuit trench isolation structure - in which trenches are filled with alternating layers of oxygen-rich oxynitride and nitrogen-rich oxynitride.
DC L03 U11
IN BERGAMI, B A; WILLIAMS, P H
PA (MOTI) MOTOROLA INC
CYC 1
PI US 4855804 A 19890808 (198939)* 12p <--
ADT US 4855804 A US 1988-271145 19881114
PRAI US 1987-122091 19871117; US 1988-271145 19881114; US 1988-290809 19881223
IC H01L027-12; H01L029-06
AB US 4855804 A UPAB: 19930923
Electronic device having dielectric filled trenches comprises: a substrate; first trench(es) having a first width; and second trench(es) of second width greater than the first, at least the second trench(es) being coated with alternating layers of odd numbered layers of O2-rich oxynitride and even numbered layers of N2-rich oxynitride.

The layers have alternating etch rates and each layer is thicker than a natural oxynitride interfacial layer formed between SiO2 and Si3N4.

ADVANTAGE - Isolation trenches of different widths are filled with min. mid-trench crevices or gaps and with min. substrate expansion differential, using a single deposition reactor; the layers also provide a planar surface.
3/6

L22 ANSWER 1 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:564326 HCAPLUS
DN 129:183089
TI Semiconductor device with high breakdown voltage
IN Uenishi, Akio; Minato, Tadaharu
PA Mitsubishi Denki K. K., Japan
SO Ger. Offen., 64 pp.
CODEN: GWXXBX
DT Patent
LA German
IC ICM H01L029-78
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19736981	A1	19980820	DE 1997-19736981	19970825
	DE 19736981	C2	19990826		
	JP 10223896	A2	19980821	JP 1997-26997	19970210
	US 6040600	A	20000321	US 1997-909411	19970811
	US 6103578	A	20000815	US 1999-283751	19990402 <--
PRAI	JP 1997-26997	A	19970210		
	US 1997-909411	A1	19970811		

AB N- and p-diffusion regions are formed in a region between trenches in the surface of a semiconductor substrate. A p-well is formed in the n- and p-diffusion regions near the surface. A source n+-diffusion region is formed within the p-well. A gate electrode layer is formed between the n-diffusion region and the source n+-diffusion region with an intermediate gate insulator layer. The n- and p-diffusion regions each have a dopant concn. distribution which is diffused from 1 sidewall of a trench. Thus a fine p-n repetition structure of the order of .mu.m is obtained with excellent precision and a semiconductor device with high breakdown voltage is prepd.

ST semiconductor device high breakdown voltage

L22 ANSWER 2 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:595076 HCAPLUS
DN 127:184367
TI Field effect-controlled semiconductor devices
IN Tihanyi, Jenoe
PA Siemens A.-G., Germany
SO Ger. Offen., 10 pp.
CODEN: GWXXBX
DT Patent
LA German
IC ICM H01L029-78
ICS H01L029-739
CC 76-3 (Electric Phenomena)
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI	DE 19604043	A1	19970807	DE 1996-19604043	19960205	
	DE 19604043	C2	20011129			
	WO 9729518	A1	19970814	WO 1997-DE182	19970130	
	W: CN, JP, KR, US					
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE					
	EP 879481	A1	19981125	EP 1997-907035	19970130	
	EP 879481	B1	20020502			
	R: DE, FR, GB, IT, IE					
	JP 2000504879	T2	20000418	JP 1997-528039	19970130	
	EP 1039548	A2	20000927	EP 2000-112818	19970130	
	EP 1039548	A3	20010117			
	R: DE, FR, GB, IT, IE					
	US 6176121	B1	20010123	US 1997-875708	19970804	
	US 6184555	B1	20010206	US 1998-117636	19981204	<--
PRAI	DE 1995-19504814	A	19950214			
	WO 1995-EP3294	W	19950818			
	DE 1996-19604043	A	19960205			
	DE 1996-19604044	A	19960205			
	EP 1997-907035	A3	19970130			
	WO 1997-DE182	W	19970130			

AB The devices, comprising a drain region of a 1st type of cond., .gtoreq.1 polycryst. Si gate electrodes insulated from the drain region, .gtoreq.1 source regions of a 2nd type of cond. in the drain region, comprise regions of the 1st and 2nd cond. formed in the drain region, and the total amt. of dopants of the n-regions formed is approx. equal to the total amt. of dopant of the p-regions formed.
ST field effect control semiconductor device; n p type semiconductor
IT Semiconductor devices

L22 ANSWER 4 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1998-448367 [39] WPIX
DNN N1998-349568
TI Semiconductor component of low loss and high breakdown voltage - has semiconductor substrate with two opposite main surfaces and numerous grooves in first surface.
DC U12
IN MINATO, T; UENISHI, A
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 3
PI DE 19736981 A1 19980820 (199839)* 64p H01L029-78
JP 10223896 A 19980821 (199844) 28p H01L029-78
DE 19736981 C2 19990826 (199938) H01L029-78
US 6040600 A 20000321 (200021) H01L029-78
US 6103578 A 20000815 (200041) H01L021-336 <--
ADT DE 19736981 A1 DE 1997-19736981 19970825; JP 10223896 A JP 1997-26997 19970210; DE 19736981 C2 DE 1997-19736981 19970825; US 6040600 A US 1997-909411 19970811; US 6103578 A Cont of US 1997-909411 19970811, US 1999-283751 19990402
PRAI JP 1997-26997 19970210
IC ICM H01L021-336; H01L029-78
AB DE 19736981 A UPAB: 19981001
The component has a first doping region (1) of a first conductivity-type formed within a substrate region between two grooves (7a) in laminated structure and a side wall face of one groove. A second doping region (2) is similarly formed with respect to the second groove, is of second conductivity-type and forms with the first region of a PN-junction.

A second conductivity-type third doping region (3) is formed nearer to the first main surface. A fourth doping region (5) of first conductivity type is at least at the first main surface, or a side wall face of a groove (7) such that it is opposite to the first region. Opposite to the third region is located a gate electrode layer (9) with an intermediate gate insulating film (8). The first and second region have specified concentration distribution.

USE/ADVANTAGE - For switching current sources, inverters. Fine PN-repeat structure, enabling high breakdown voltage.

Dwg.1/66
FS EPI

L28 ANSWER 6 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2001-061615 [07] WPIX
DNN N2001-046181 DNC C2001-017134
TI Power semiconductor device for high power applications in, e.g. motor drive circuit, includes an electrically insulating region on a sidewall of a trench.
DC L03 U11 U12
IN BALIGA, B J
PA (MICR-N) MICRO-OHM CORP; (BALI-I) BALIGA B J
CYC 94
PI WO 2000074146 A1 20001207 (200107)* EN 60p H01L029-872
US 6191447 B1 20010220 (200112) H01L029-76
US 2001000033 A1 20010315 (200116) H01L021-8232
AU 2000051730 A 20001218 (200118) H01L029-872
US 6365462 B2 20020402 (200226) H01L021-336
EP 1198843 A1 20020424 (200235) EN H01L029-872
AB WO 200074146 A UPAB: 20010508
NOVELTY - Power semiconductor device comprises a substrate, a first trench in the substrate, an electrically insulating region on a sidewall of the trench, and an electrode on the tapered sidewall of the insulating region. The insulating region has a tapered sidewall that extends outwardly relative to a bottom of the trench at an average slope of 500-1500 Angstrom / microns relative to the sidewall of the trench.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming the power semiconductor device, i.e. UMOSFET.

USE - For high power applications in motor drive circuit, appliance controls, and robotics and lighting ballasts.

ADVANTAGE - The device has low on-state resistance and high blocking voltage capability.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the Schottky barrier rectifiers.

Dwg.14/20
TECH WO 200074146 A1UPTX: 20010202
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Device: The substrate comprises a drift region of a first conductivity type. A portion of the drift region extends opposite the sidewall of the trench and is uniformly doped with first conductivity type dopants at a level not less than 1 x 1017 cm-3. The device further comprises a second trench, a base region of a second conductivity type in the substrate, a source region of a first conductivity type. The first and second **trenches** define a drift region mesa in between. The product of a width of the drift region mesa and the first conductivity type dopant concentration in the first portion of the drift region is 5 x 1012-7.5 x 1012 cm-2. The drift region extends to a surface of the substrate, and the electrode extends onto the surface and forms a Schottky rectifying junction with the drift region. The base region forms a first P-N rectifying junction with the drift region that extends to the sidewall of the first trench. The source region forms a second P-N rectifying junction with the base region that extends to the sidewall of the first trench. The sidewall of the first trench defines an interface between the drift region and the insulating region, and an interface between the base region and insulating region. The tapered sidewall of the insulating region extends opposite the base region. The first thickness of the insulating region is greater than a second thickness of the insulating region at a location extending opposite the second P-N rectifying junction.

L30 ANSWER 4 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1989-326283 [45] WPIX
DNN N1989-248365 DNC C1989-144428
TI Symmetrical blocking high voltage breakdown semiconductor device - with a lower **junction** terminal brought to the upper surface.
DC A85 L03 U12
IN TEMPLE, V A
PA (GENE) GENERAL ELECTRIC CO; (HARO) HARRIS CORP
CYC 6
PI EP 341075 A 19891108 (198945)* EN 12p
R: DE FR IT NL
JP 02022869 A 19900125 (199010)
US 4904609 A 19900227 (199015)
US 4999684 A 19910312 (199113)
EP 341075 B1 19960417 (199620) EN 16p H01L029-866
R: DE FR IT NL
DE 68926261 E 19960523 (199626) H01L029-866
AB EP 341075 A UPAB: 19960129
Fabrication method of a symmetrical blocking, high breakdown voltage, semiconductor device is new. Mfr., with reference to the figure (1) comprises using a semiconductor substrate (14) of a first conductivity type having an epitaxial layer (16) of a second conductivity type. First and second **laterally** spaced regions of the first conductivity type (20, 22) are formed in an upper surface of the epitaxial layer to form repsectively first and second PN **junctions**. A groove (60) having a sloped sidewall is formed in the second region which extends from the upper surface, through epitaxial layer and into the substrate. Impurities of a first conductivity type are implanted into the side walls, of the groove to form a thin layer (64). The deice is annealed to activate the impurities so that the implanted layer (64) electrically connects the second region (22) to the substrate.

USE/ADVANTAGE - A simple and convenient method for bringing the reverse voltage blocking **junction** to a termination at the device surface. Complete fabrication of a plurality of devices is possible, prior to each individual die being broken out of the wafer.

1E/2

Dwg.1E/2

ABEQ US 4904609 A UPAB: 19930923
Symmetrical blocking high breakdown voltage semiconductor device is produce by firstly providing a substrate of semiconductor material of a first conductivity type having on it an epitaxial layer (I) of a second conductivity type. First and second, **laterally** spaced regions of the first conductivity type are formed in an upper surface of layer (I), the first and second regions forming, with layer (I), respective first and second PN **junctions**.

A groove is formed having a sloped sidewall in the second region, the groove extending from the upper surface, through the second region and layer (I), into the substrate. Impurities of the first conductivity type are implanted into the sidewall of the groove, to form a thin implanted layer of the first conductivity type. Finally, the device is annealed sufficiently to activate the impurities in the implanted layer to form a low resistivity path that electrically connects the second region to the substrate.

ADVANTAGE - The reverse voltage blocking **junction** in semiconductor devices contg. PNP structures is brought to the top surface of the wafer. @@

ABEQ US 4999684 A UPAB: 19930923
Device comprises a 1st conductivity type substrate; a 2nd conductivity type epitaxial layer; a main region of 1st type extending into the epitaxial layer from its upper surface; a sec. region of 1st type extending into the epitaxial layer from its upper surface and surrounding the main region, this sec. region spaced from the main region and having a

sloped sidewall surface which extends from the upper surface of the epitaxial layer through the sec. region and epitaxial layer and into the substrate; the main and sec. regions forming respective PN **junctions** with the epitaxial layer; and a thin implanted layer of 1st type impurities in the sloped sidewall surface forming a low resistivity path to electrically connect the sec. region to the substrate. A means is between the main and sec. regions to control the symmetrical blocking and breakdown voltage of the device comprising a 1st **junction** termination extension comprising a 1st type region extending **laterally** from the main region toward the sec. region, and a 2nd **junction** termination extension comprising a 1st type region extending **laterally** from the sec. region toward the 1st extension. A field stop region is between each extension.

ADVANTAGE - Relatively simple construction, having symmetrical blocking and voltage breakdown characteristics. The device can be mass produced.

ABEQ EP 341075 B UPAB: 19960520

A semiconductor device comprising a semiconductor substrate (14; 88) of a first conductivity type; an epitaxial layer (16; 90) of a second conductivity type disposed on the substrate (14; 88) a main region (20; 94) of the first conductivity type extending into said epitaxial layer (16; 90) from an upper surface (18; 92) thereof; a sloped sidewall (62) extending from the upper surface (18; 92(of the said epitaxial layer (16; 90) through the epitaxial layer and into the substrate (14; 88); and a thin implanted layer of impurities of the first conductivity type (64,140) in the sloped sidewall (82), which semiconductor device is characterised by being a symmetrical blocking high breakdown voltage semiconductor device further comprising a secondary region (22; 98) of the first conductivity type extending into said epitaxial layer (16; 90) from the upper surface (18; 92) thereof and surrounding the main region (20; 94), said secondary region (22; 98) being spaced from said main region (20; 94), the sloped sidewall (62) extending through the secondary region (22; 98) so that the thin implanted layer of impurities of the first conductivity type (64,140) forms a low resistivity path for electrically connecting the secondary region (22; 98) to the substrate (14; 88).

Dwg.1A/2D

FS CPI EPI

FA AB

L30 ANSWER 5 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1986-015153 [03] WPIX
DNN N1986-011129
TI Power JFET with multiple **lateral** pinching - has main terminals coupled to one end of channels and gate terminals to layers of opposite conductivity.
DC U12 U24
IN BENJAMIN, J A; LADE, R W; SCHUTTEN, H P
PA (EAYT) EATON CORP
CYC 5
PI EP 167810 A 19860115 (198603)* EN 14p
R: DE FR GB NL
JP 61046077 A 19860306 (198616)
ADT EP 167810 A EP 1985-106859 19850604
PRAI **US 1984-618434 19840608**
REP 1.Jnl.Ref; DE 2728532; DE 3345189; EP 53854; EP 83815; FR 1306187; FR 1377330; FR 2152656; FR 2454703
IC H01L029-80
AB EP 167810 A UPAB: 19930922
The device has a row of alternating conductivity type layers forming a number of channels and has an ON state conducting bidirectional current horizontally longitudinally through the channels. The device has an OFF state blocking current flow through the channels due to horizontally **lateral** depletion pinch-off. The layers extend vertically and horizontally longitudinally and the direction of layering extends horizontally **laterally**.

Main terminals are coupled to one end of the channels and gate terminals are coupled to the layers having opposite conductivity to the channels. A depletion region spreads from the **junctions** of the layer causing the pinch-off OFF state and shrinks back to enable the ON state.

USE/ADVANTAGE - Use includes AC power applications. Multiple channels reduce ON state resistance/linear geometry enables desirable control of breakdown voltage and high blocking voltage capability.

L30 ANSWER 6 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1985-312018 [50] WPIX
DNN N1985-231670
TI **Lateral** bidirectional power MOSFET - has common drift region between stacks of channel-containing regions interleaved with source regions and channel-gating devices.
DC U12
IN BENJAMIN, J A; LADE, R W; SCHUTTEN, H P
PA (EAYT) EATON CORP
CYC 6
PI EP 164096 A 19851211 (198550)* EN 15p
R: DE FR GB NL
JP 61172373 A 19860804 (198637)
US 4622569 A 19861111 (198648)
ADT JP 61172373 A JP 1985-125011 19850608; US 4622569 A US 1984-618537 19840608
PRAI **US 1984-618537 19840608**
REP A3...8702; EP 53854; EP 91686; EP 97442; No-SR.Pub
IC H01L029-78
AB EP 164096 A UPAB: 19930925
Channel-containing regions (12-14) of a first stack are interleaved with source regions (15-17), and in a second stack (10) a second number source regions (21-23) are interleaved with other channel-containing regions (18-20). A device (24) for gating on the channels to invert their conductivity type includes a dielectric layer (30) and gate electrode (32) which are arranged adjacent to the channels (12a-14a,18a-20a) to provide electric fields of a field strength which is effective to achieve the conductivity inversion required.

Application to the gate terminal (G) of a positive potential attracts electrons from a channel-containing region (12) to invert the conductivity in the region (12a) so that an n-type conduction channel (12a) is formed between the n-type source regions (15,16). Voltage applied between source regions (15,21) of the respective first, and second stack (8,10) produces a flow of current between them through the induced conduction channels and the common drift region (6).

USE/ADVANTAGE - Bidirectional power switching, including AC application. Construction achieves enhanced voltage blocking in off state.

1/3
ABEQ US 4622569 A UPAB: 19930925
The FET (2) has a common drift region (6) between first and second stacks (8,10) of alternating conductivity type layers (12-17 and 18-23). A notch (38) extends vertically downwardly into the drift region. The stacks include channel-containing regions (12-14 and 18-20) interlayed with source regions (15-17 and 21-23).

In the ON state, bidirectional current flows serially through the source regions and channels of each stack and through the drift region. In the OFF state, voltage is dropped across the **junctions** in series in the stacks, and the respective **junctions** with the drift region.

3/3
FS EPI

L30 ANSWER 7 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1985-312017 [50] WPIX
DNN N1985-231669
TI Vertical bidirectional multi-channel stacked power MOSFET - has downwardly extending notch including insulated gate electrode for inverting conductivity of channel-containing regions.
DC U12
IN BANJAMIN, J A; LADE, R W; SCHUTTEN, H P
PA (EAYT) EATON CORP
CYC 5
PI EP 164095 A 19851211 (198550)* EN 11p
R: DE FR GB NL
JP 61046071 A 19860306 (198616)
PRAI **US 1984-618443 19840608**
REP 1.Jnl.Ref; A3...8701; EP 53854; EP 91686; EP 97442; JP 55133574; No-SR.Pub
IC H01L029-78
AB EP 164095 A UPAB: 19930925
Several alternating conductivity type layers extend **laterally** and horizontally, and are stacked vertically top and bottom major surfaces (44,46). The stack (48) includes a number of channel-containing regions (49-54) interleaved with several source regions (55-61). A notch (70) extends downwardly through the lowermost channel-containing region of the stack, and includes an insulated gate electrode (68), for inverting the conductivity type of the regions. This induces conduction channels (49a-54a) between the source regions and enables bidirectional field effect current conduction between the top and bottom surfaces.

OFF state voltage is dropped in each direction serially across the **junctions** between the layers so that the depletion region spreading from a number of **junctions** must be vertically coupled before OFF state breakdown.

ADVANTAGE - Negative bias prevents attraction of electrons toward notch in OFF state so preventing unwanted inducement of conduction channels.

3/3
FS EPI

L115 ANSWER 16 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 1984-277851 [45] WPIX
DNN N1984-207424 DNC C1984-117769
TI Semiconductor device mfr - with insulating walls forming islets, mfd in two steps.
DC L03 U11 U12
IN VERTONGEN, B; VITE, J L
PA (PHIG) RTC RADIOTECHNIQUE COMPELEC
CYC 6
PI FR 2543739 A 19841005 (198445)* 13p
EP 126499 A 19841128 (198448) FR
R: DE FR GB NL
JP 59182565 A 19841017 (198448)
CA 1215480 A 19861216 (198703)
EP 126499 B 19880113 (198802) FR
R: DE FR GB NL
DE 3468781 G 19880218 (198808)
JP 05023054 B 19930331 (199316) 7p H01L021-331
AB FR 2543739 A UPAB: 19930925
Process for mfg. a semiconductor device including at least one high voltage bipolar transistor from at least three superposed epitaxial layers (2,3,7) of alternate conductivity types constituting in succession, the collector base and emitter of the transistor and deposited on a substrate (1) acting as a support, the device being enclosed in a box, the side insulating walls (6) of which, being of the same conductivity type as the surface epitaxial layer (7) and the deepest epitaxial layer (2), penetrate into the layer (2) after having crossed the intermediate epitaxial layer (3), is claimed.

The thickness and concn. of the surface layer (7) are such that on applying an inverse voltage between this and the intermediate layer (3), the deserted zone engendered by this voltage extends into the deepest layer (2) for a voltage below the breakdown voltage of the isolation **junction** created along the **side** walls (6); and the distance sepg. the side insulating walls (6) from the contact islands (10) of the intermediate layer is greater than the width of the deserted zone around the isolating **junction**.

The side walls (6) are formed in at least 2 steps; a first part (6a) being created before the deposition of the epitaxial surface layer (7) from the surface of the intermediate layer; and a second portion (6b) being created facing the first part (6a) after deposition of layer (7) from the surface.

The presence of side insulating walls provides a stronger structure than the fragile insulating furrows of prior art. The procedure described above permits application of the ''**Resurf**'' (RTM) procedure unlike other prior art processes where insulating walls are used to form islands.

5/5

ABEQ EP 126499 B UPAB: 19930925
A method of manufacturing s semiconductor device comprising at least one high-voltage bipolar transistor, according to which method there are successively deposited on a substrate (1) a first epitaxial layer (2) of a first conductivity type and a second epitaxial layer (3) of the second conductivity type opposite to the first type, a contact zone (10) is formed on the second epitaxial layer (3) and lateral isolating separation walls (6) of the first conductivity type are formed, these separation walls penetrating into the first epitaxial layer after having traversed the second epitaxial layer (3), the said lateral separation walls (6) surrounding an island formed in the second epitaxial layer (3), the thickness and the doping concentration of the second layer (3) being such that, when an inverse voltage is applied to the pn-**junction** between on the one hand the second epitaxial layer (3) and on the other hand the first epitaxial layer (2) and the isolating separation walls (6),

the **depleted** zone produced by this voltage extends throughout the thickness of the second epitaxial layer (3) for a value of the said voltage lower than the breakdown voltage, the distance between the lateral isolating separation walls (6) and the contact zone (10) being larger than the maximum lateral extend of the **depleted** zone from the isolating separation walls (6) in the second epitaxial layer (3), characterised in that third epitaxial layer (7) of the first conductivity type is deposited on the second epitaxial layer (3), in that the isolating separation walls (6) are manufactured in at least two stages, a first portion (6a) being formed before the deposition of the third epitaxial layer (7) and extending through at least the whole thickness of the second layer (3), and a second portion (6b) being formed opposite to the first portion (6a) after the deposition of the third layer (7) and throughout the thickness of the latter, and in that a part of the third epitaxial layer (7) situated w

FS CPI EPI

FA AB

L115 ANSWER 6 OF 22 INSPEC COPYRIGHT 2002 IEE
AN 2000:6468048 INSPEC DN B2000-02-2560R-069
TI Analysis of the effect of charge imbalance on the static and dynamic characteristics of the **super junction** MOSFET.
AU Shenoy, P.M.; Bhalla, A.; Dolny, G.M. (Ind. Power Product Dev., Harris Semicond., Mountaintop, PA, USA)
SO 11th International Symposium on Power Semiconductor Devices and ICs. ISPSD'99 Proceedings (Cat. No.99CH36312)
Piscataway, NJ, USA: IEEE, 1999. p.99-102 of xxiii+359 pp. 6 refs.
Conference: Toronto, Ont., Canada, 26-28 May 1999
Sponsor(s): IEEE Electron Devices Soc.; Inst. Elec. Eng. of Japan
Price: CCCC 0 7803 5290 4/99/$10.00
ISBN: 0-7803-5290-4
DT Conference Article
TC Practical; Theoretical
CY United States
LA English
AB In this paper, a novel device called the **super junction** MOSFET is analyzed using analytical modeling and numerical simulations. The effect of charge imbalance between the N and P pillars on the static and dynamic characteristics of the device is studied in detail. Simulations predict that this device is highly sensitive to charge imbalance if designed for optimum on-resistance. The breakdown voltage (**BV**) and Eoff sensitivity can be reduced considerably by degrading the specific on-resistance Ron,sp. The physics of the static and dynamic behaviour of this device under charge imbalance is explained with the help of numerical simulations.
CC B2560R Insulated gate field effect transistors; B2560P Power

L115 ANSWER 7 OF 22 INSPEC COPYRIGHT 2002 IEE
AN 1989:3297170 INSPEC DN B89009348
TI Modeling and optimization of lateral high voltage IC devices to minimize 3-D effects.
AU Yilmaz, H. (Res. & Dev. Eng., Semicond. Bus. Div., General Electr. Co., Research Triangle Park, NC, USA)
SO Proceedings of the Symposium on High Voltage and Smart Power Devices
Editor(s): Shackle, P.
Pennington, NJ, USA: Electrochem. Soc, 1987. p.290-4 of 356 pp. 7 refs.
Conference: Philadelphia, PA, USA, Spring 1987
DT Conference Article
TC Theoretical
CY United States
LA English
AB The high **voltage blocking** capability of the **reduced surface field** or **lateral** charge control (LCC) devices are strongly **junction** curvature dependent. A new charge model has been developed to translate the 3D curvature effect into a 2D plane. An existing 2D computer program in conjunction with this new model has been utilized to model and optimize the LCC devices for high voltage ICs. Theoretical predictions of this model are within 10% of measured results.
CC B2570 Semiconductor integrated circuits; B2560B Modelling and equivalent

L115 ANSWER 21 OF 22 JAPIO COPYRIGHT 2002 JPO
AN 1991-150877 JAPIO
TI MANUFACTURE OF LENS-SHAPED LIGHT EMITTING DIODE
IN IZUMI ITARU
PA SHARP CORP, JP (CO 000504)
PI JP 03150877 A 19910627 Heisei
AI JP1989-289612 (JP01289612 Heisei) 19891107
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1115, Vol. 15, No. 379, P. 49 (19910925)
IC ICM (5) H01L033-00
AB PURPOSE: To facilitate manufacture of a homoepitaxy-type lens-shaped light emitting diode and reduce the cost of the diode by a method wherein rows of protrusions having lens-shaped cross sections are formed on one of the surfaces of a substrate by dicing and two epitaxial layers which are of the same type as the substrate and which form a **P-N** junction between each other are formed on the surface.
CONSTITUTION: Rows of protrusions 2 having lens-shaped cross sections are formed on one of the surfaces of an **N**-type GaP substrate 1 by forming **trenches** with a pitch corresponding to the **chip** size by dicing. Then an **N**-type and **P**-type epitaxial layers 3 and 4 made of GaP crystal of which the substrate 1 is also made are successively formed by a liquid epitaxial growth method to form a **junction** part 5. **P**-type **side** electrodes 6 of the **chips** are formed on the center parts of the respective regions surrounded by the dicing **trenches** and **N**-type **side** electrodes 7 are formed on the rears of the respective regions. The substrate 1 is cut along the dicing **trenches** into the individual **chips**. With this constitution, a homoepitaxy-type lens-shaped light emitting diode can be manufactured at a low cost.